

**525.412 Computer Architecture Syllabus**  
**Fall 2011**

Engineering for Professionals  
Whiting School of Engineering  
Johns Hopkins University  
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Date	Lesson	Topics
31-Aug-11	Introduction	History of Computer Architecture Overview of Modern Computer Architecture RISC v. CISC Parallel computing Primary & secondary memor Input and Output
07-Sep-11	Review	Digital design Logic gates Flip-flops and register Decoders and encoder Multiplexers and demultiplexer Memory systems Design at the gate, register, and processor levels
14-Sep-11	Processor design I	<b>Quiz 1</b> Instruction formats Classes of instructions Addressing modes Immediate, register, direct, indirect, indexed, based-index, stack, relative Datapath design Control design Instruction-level parallelism Resets, exceptions, interrupts, traps, and system calls Microprogramming
21-Sep-11	Processor design II	
28-Sep-11	Processor design III	<b>Quiz 2</b>
05-Oct-11	Computer arithmetic	Number representation 1's & 2's complement, BCD, excess, IEEE floating point Addition and subtraction Ripple carry, look-ahead carry, excess Multiplication and division Robertson's and Booth's algorithm Restoring & non-restoring division Parallel designs Square root Converging iteration Fast computation Pipelining, parallelism, table look-up ALU design
12-Oct-11	Midterm Exam	
19-Oct-11	Software issues	O/S, assemblers, compilers, interpreters, linkers, loaders Macros Bind time Sequential processes, coroutines, procedures
26-Oct-11	Memory I	Masters and slaves; servers and clients; peer-to-peer relationships Integrated Circuit ROM, PROM, EPROM, EEPROM, Flash, RAM, magnetic bubble Associative Disk, tape, optical, mass storage RAID Memory access Hierarchical, cache, segmented, virtual Address translation Error detection and correction

<b>Date</b>	<b>Lesson</b>	<b>Topics</b>
<b>02-Nov-11</b>	Memory II	<b>Quiz 3</b>
<b>09-Nov-11</b>	I/O I	Buses Bus width, contention, arbitration Control, data, address Handshaking Programmed v. interrupt-drive Priority DMA Serial v. parallel IDE, SCSI, PCI, USB, Firewire
<b>16-Nov-11</b>	I/O II	
<b>23-Nov-11</b>	Thanksgiving	
<b>30-Nov-11</b>	High-performance computer design	<b>Quiz 4</b> Superscalar and VLIW Multiprocessors and multicomputers  Branch prediction, out-of-order execution, speculative execution SISD v. SIMD; MIMD; vector processors Practical considerations Power, temperature, mass, volume, cost, administrative overhead, execution time, queuing, communications, data volume, scaling
<b>07-Dec-11</b>	Final Exam	