

5.25 GHz Low Noise Amplifier Using Triquint MMIC Process

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Summary

This report documents the design of a low-noise amplifier designed at 5.25 GHz using the Triquint TQS TRx process. The design was produced as a part of the MMIC Design course taught at Johns Hopkins University during the Fall 2000 semester.

The LNA was designed for use in a C-band HYPERLAN transceiver. Other designs produced in the course were to be used alongside this design as parts of this transceiver.

The design software used to design the LNA was Agilent Advanced Design System 1.3 (ADS). The elements used were custom model elements based on the Triquint process. The design was laid out on a 60 x 60 mil chip by Anachip. The final MMIC design will be fabricated and tested over the course of the first six months of 2001.

Introduction

Circuit Description

The circuit topology chosen for the design was a simple cascaded two-stage amplifier layout with self-biasing networks implemented. Matching networks were employed using lumped element topology.

Design Philosophy

In designing low-noise amplifiers, the primary goal is to maintain the lowest possible noise figure while attaining useable gain. For this design, the Triquint DFET was chosen as the transistor due to its low-noise and gain characteristics. In order to achieve the goal of 15 dB gain, a 600 um DFET was chosen over the 300 um device.

The first step in designing the LNA was to analyze the performance of the device. The DFET transistor models were nonlinear, however, they did not include noise performance. So the measured noise parameters had to be implemented in a linear model and that linear model, which provided the noise data, was used alongside the nonlinear model throughout the design process. Considering that the noise data was only taken at certain bias points, the Q-point was chosen based on the available data. The bias point chosen was

$$Vd = 2V \quad Vg = -0.225V \quad Ids = 20.85mA$$

After choosing the bias point, the S parameters, noise figure, minimum noise figure, stability, and stability circles were simulated for both the linear and nonlinear models. From this point, stabilizing inductors were added to achieve desired broadband stability.

The next point was to produce an input matching network for the first stage. This was done by matching to Γ_{opt} . Again, the nonlinear and linear models were both simulated with the matching network to verify that they were in agreement.

The second stage was identical to the first stage so the interstage matching network was derived by using the output of the first stage and the input of the first stage without the input matching network. Once again, the linear and nonlinear models were simulated in tandem.

Finally, the output matching network was derived with both stages and interstage networks in place. Initially, ideal lumped elements were used in the matching networks for quicker simulation and tweaking. Once the performance was optimized, the ideal elements were replaced with Triquint elements and re-tuned for optimum performance.

After the simplified schematic was optimized to desired performance, the layout process was initiated. For ease of layout design, all of the elements from the schematic were placed on the layout grid singly without any connection. This method made it easier to figure out spacing and routing options. Once the elements were placed on the chip in the desired locations, they were interconnected with microstrip. After the layout completion, the schematic was updated to include all of the interconnections.

As a final tweaking step, the new schematic that included the microstrip interconnects was further optimized by way of the matching networks. This was done to reclaim any performance lost during the layout generation. Any changes made after the optimization were then translated back to the layout to produce the final design.

Trade-offs

Though the DFET provided decent noise figure for the design, the stability was not within the desired range for a broadband of frequencies. Therefore, stabilization inductors had to be used on the source to provide better stability. As a consequence, the maximum gain of the device suffered.

Modeled Performance

Specification Compliance Matrix

The following table summarizes the design specifications and the corresponding simulated performance. Both the simplified schematic's and the layout schematic's performance are included in the table.

Table 1 - Specification Matrix

	Specification Goal	Simplified Schematic	Layout Schematic
Frequency Bandwidth	5150 – 5350 MHz	5150 – 5350 MHz	5150 – 5350 MHz
Gain	> 15 dB	12 dB	10.9 dB
Gain Ripple	± 0.5 dB max	± 0.05 dB	± 0.25 dB
Noise Figure	> 5 dB, 3 dB opt	2.1 dB	2.1 dB
Input IP3	> 5 dBm	-	-
VSWR, 50 ohm	< 1.5:1 input < 1.5:1 output	1.3:1 input 2.0:1 output	1.5:1 input 1.3:1 output
Supply Voltage	± 5 V, +5 only opt	+5 V	+5 V

Predicted Performance

The following plots show the performance of the design at the simplified and layout stages. Figures 1a through 1d illustrate the performance of the simplified schematic. Figures 2a through 2d illustrate the performance of the final layout schematic.

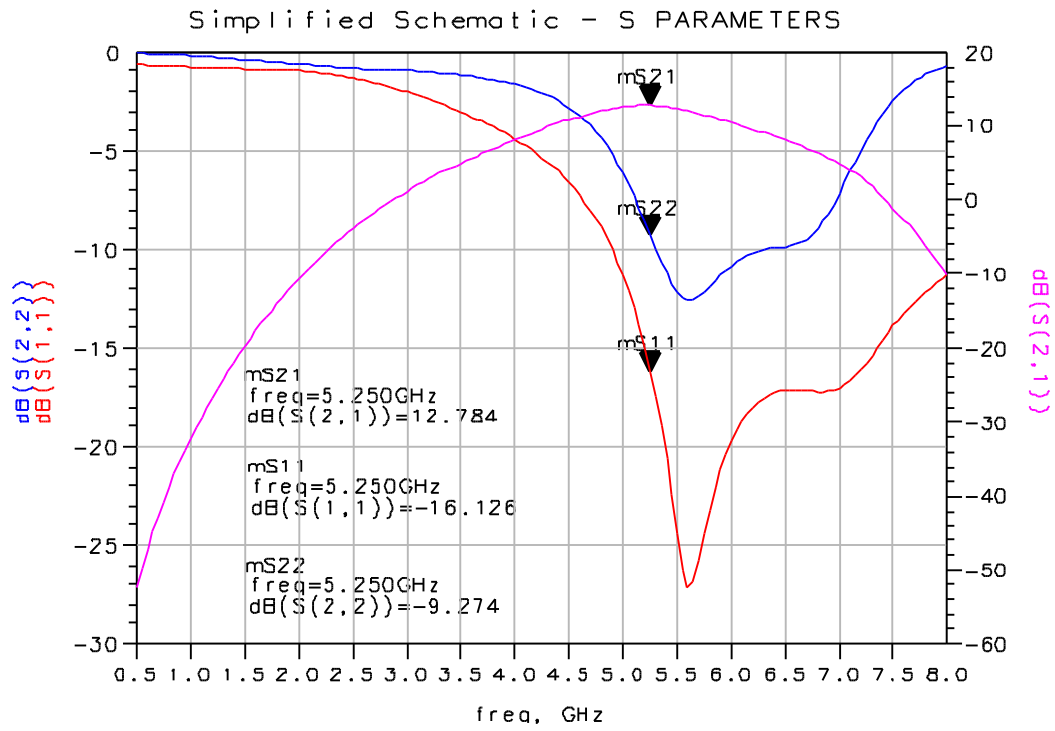


Figure 1 - simplified schematic S parameters

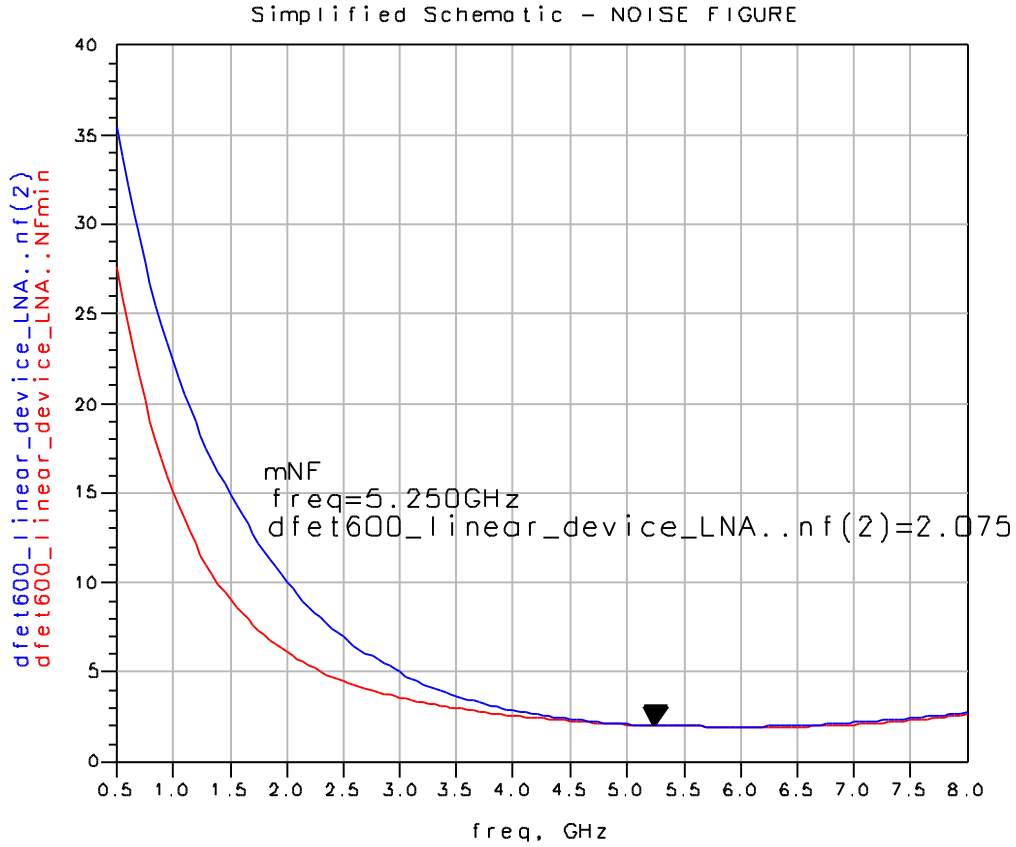


Figure 2 - simplified schematic noise figure

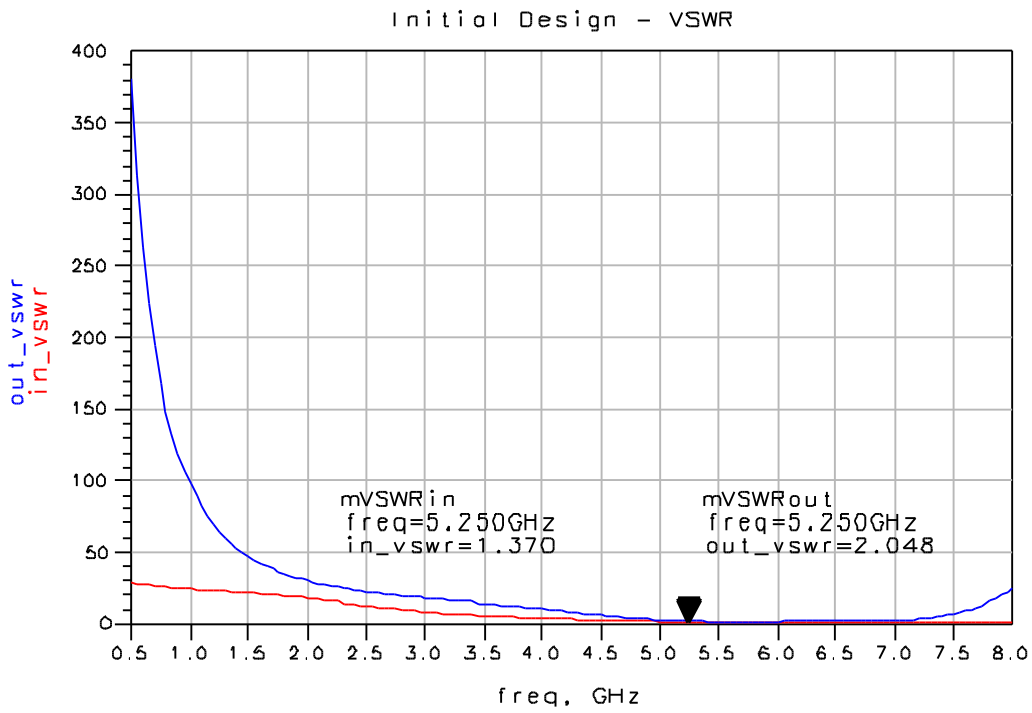


Figure 3 - simplified schematic VSWR

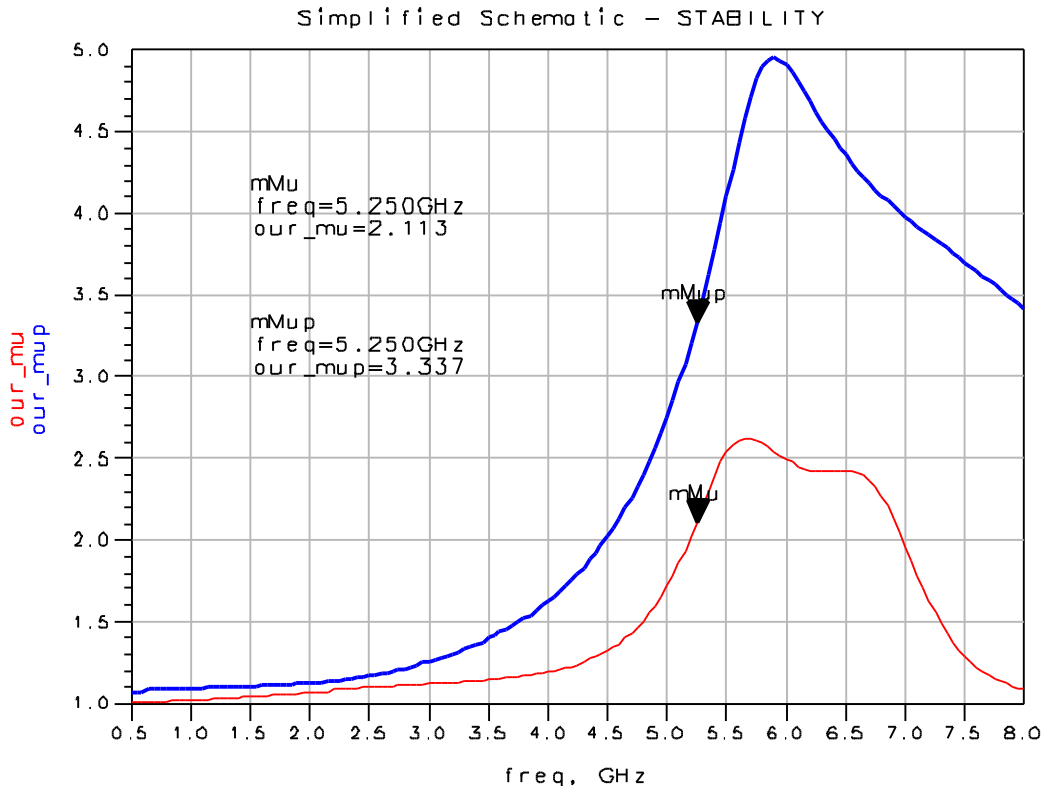


Figure 4 - simplified schematic stability

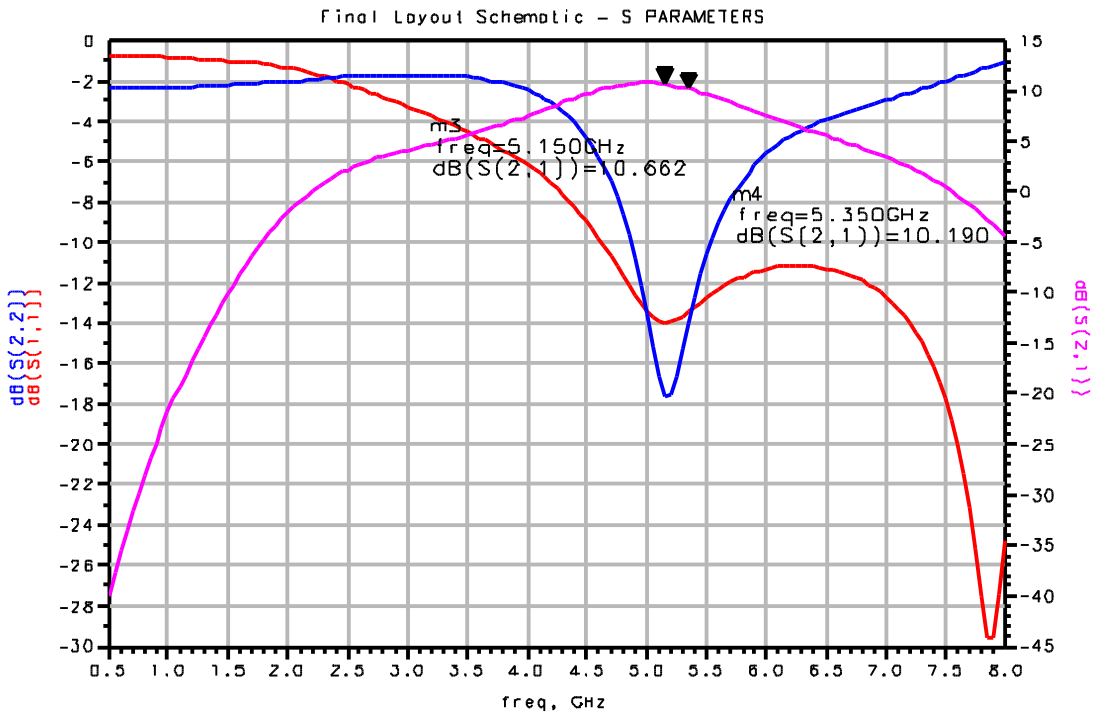


Figure 5 - final layout schematic S parameters

Final Layout Schematic - NOISE FIGURE

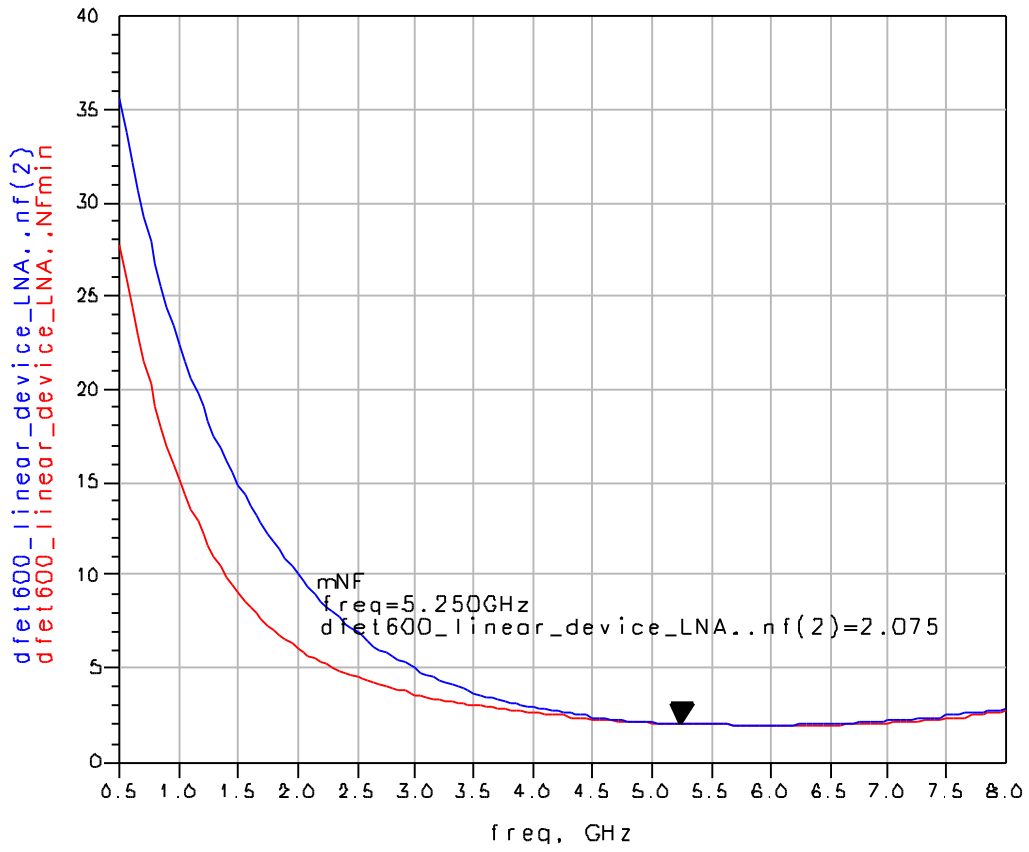


Figure 6 - final layout schematic noise figure

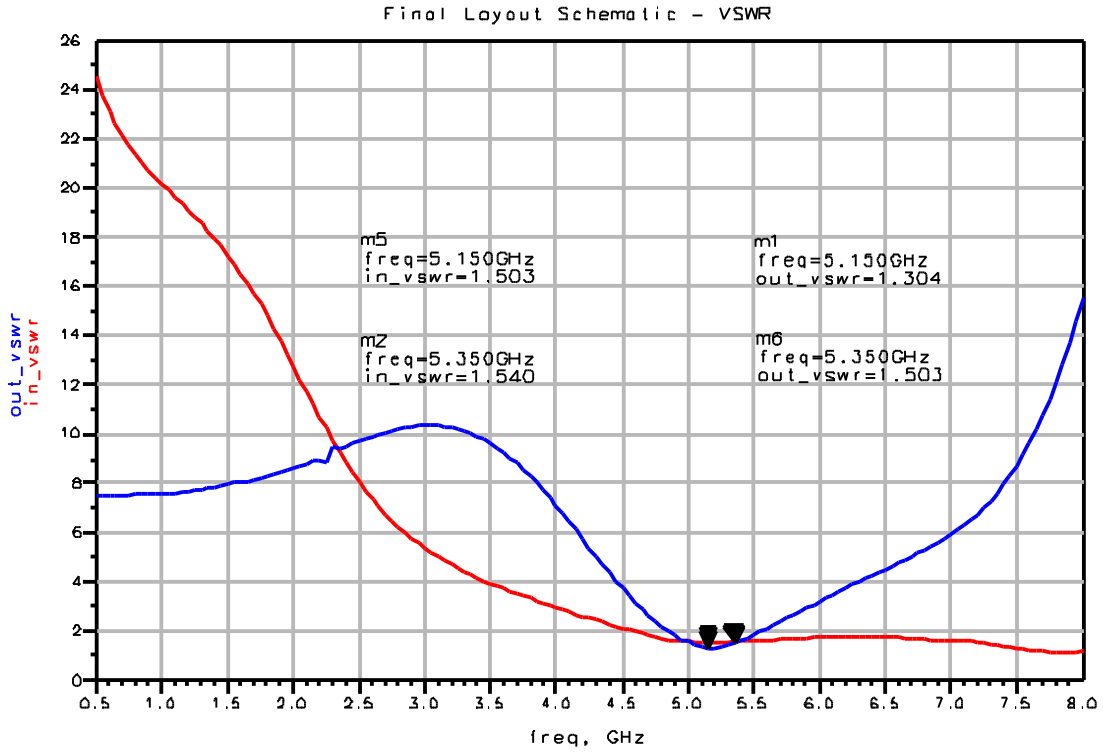


Figure 7 - final layout schematic VSWR

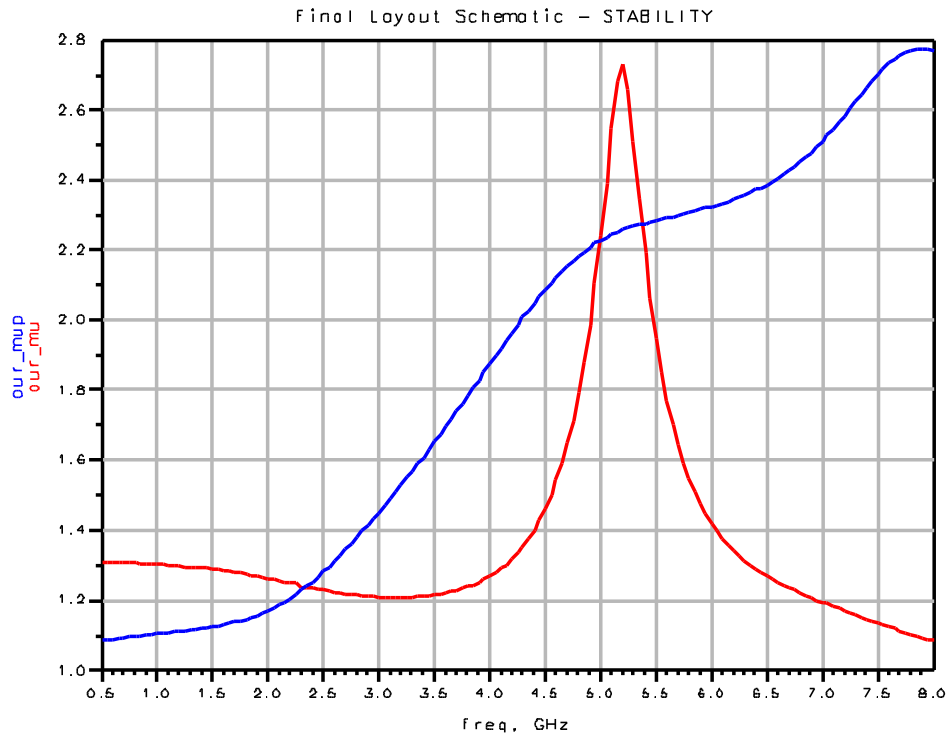


Figure 8 - final layout schematic stability

Schematic Diagrams

The following pages illustrate the final schematics used for both the simplified and layout designs.

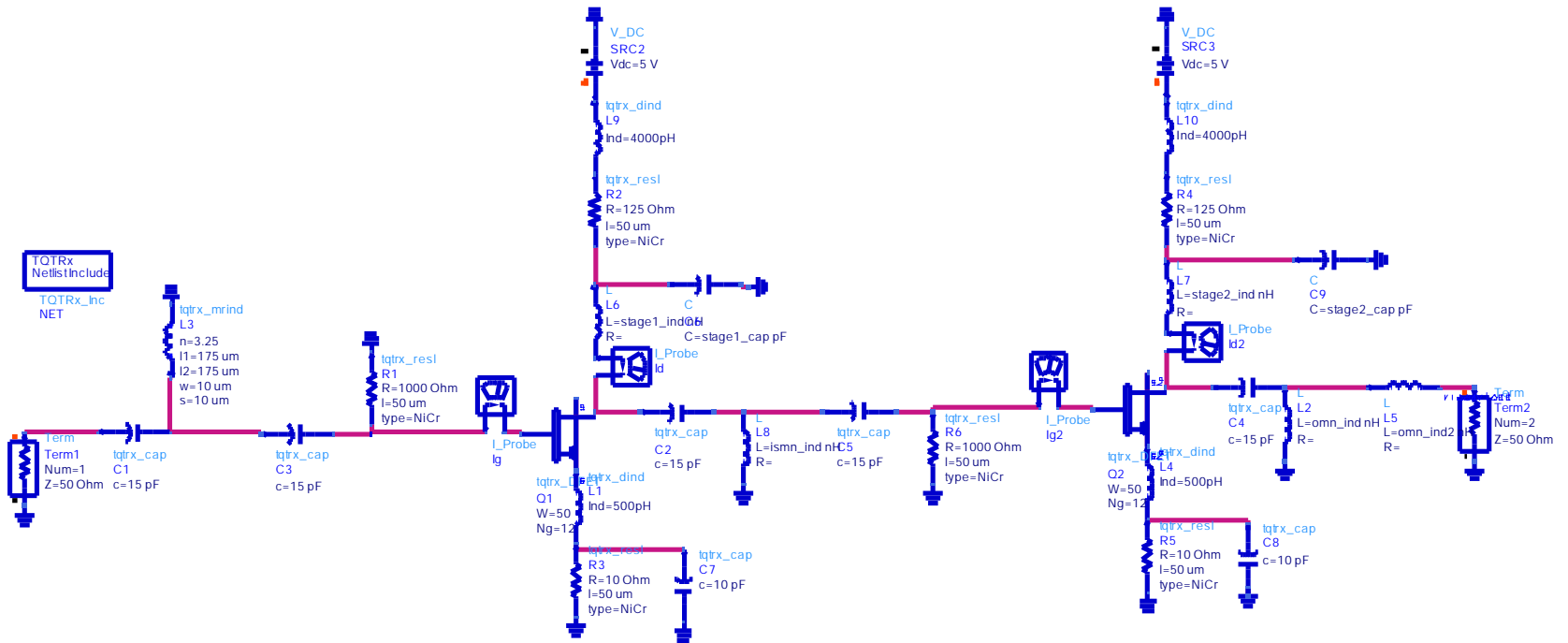


Figure 9 - simplified schematic design

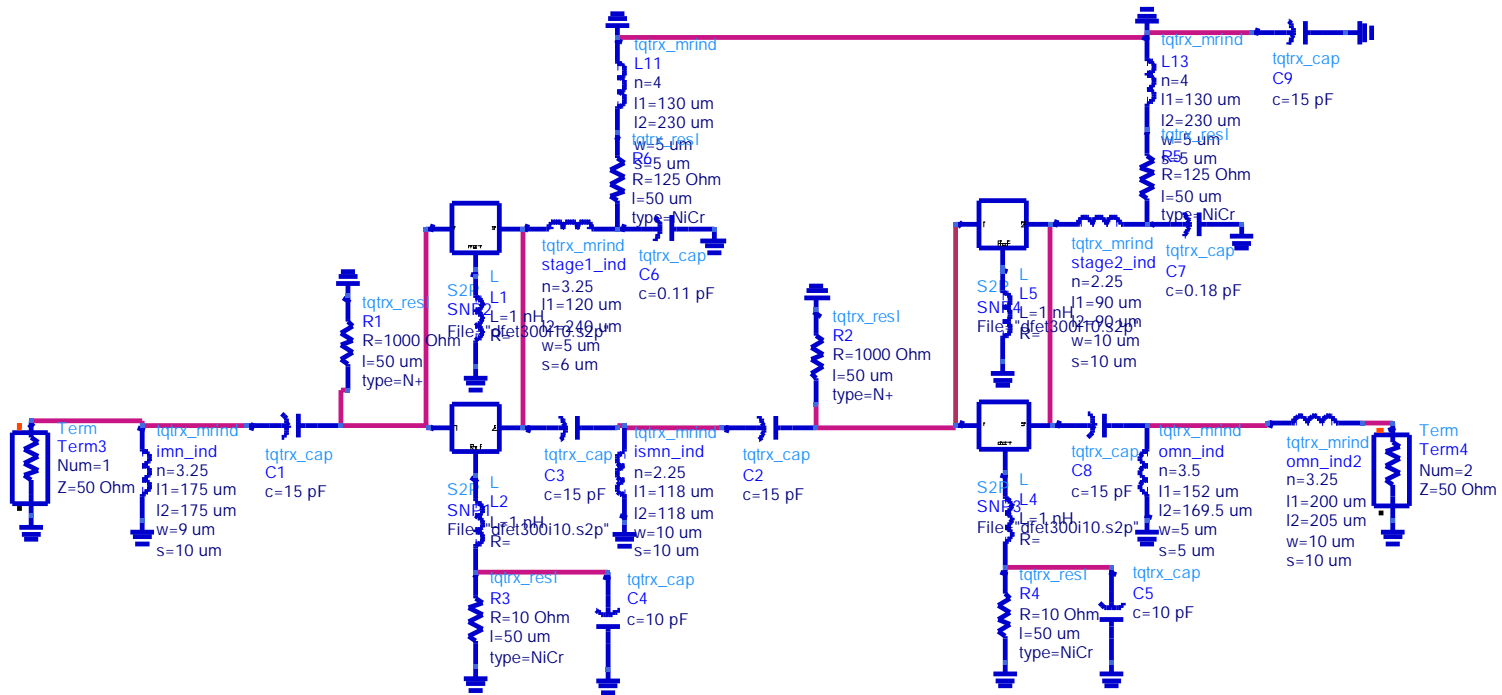


Figure 10 - linear model schematic

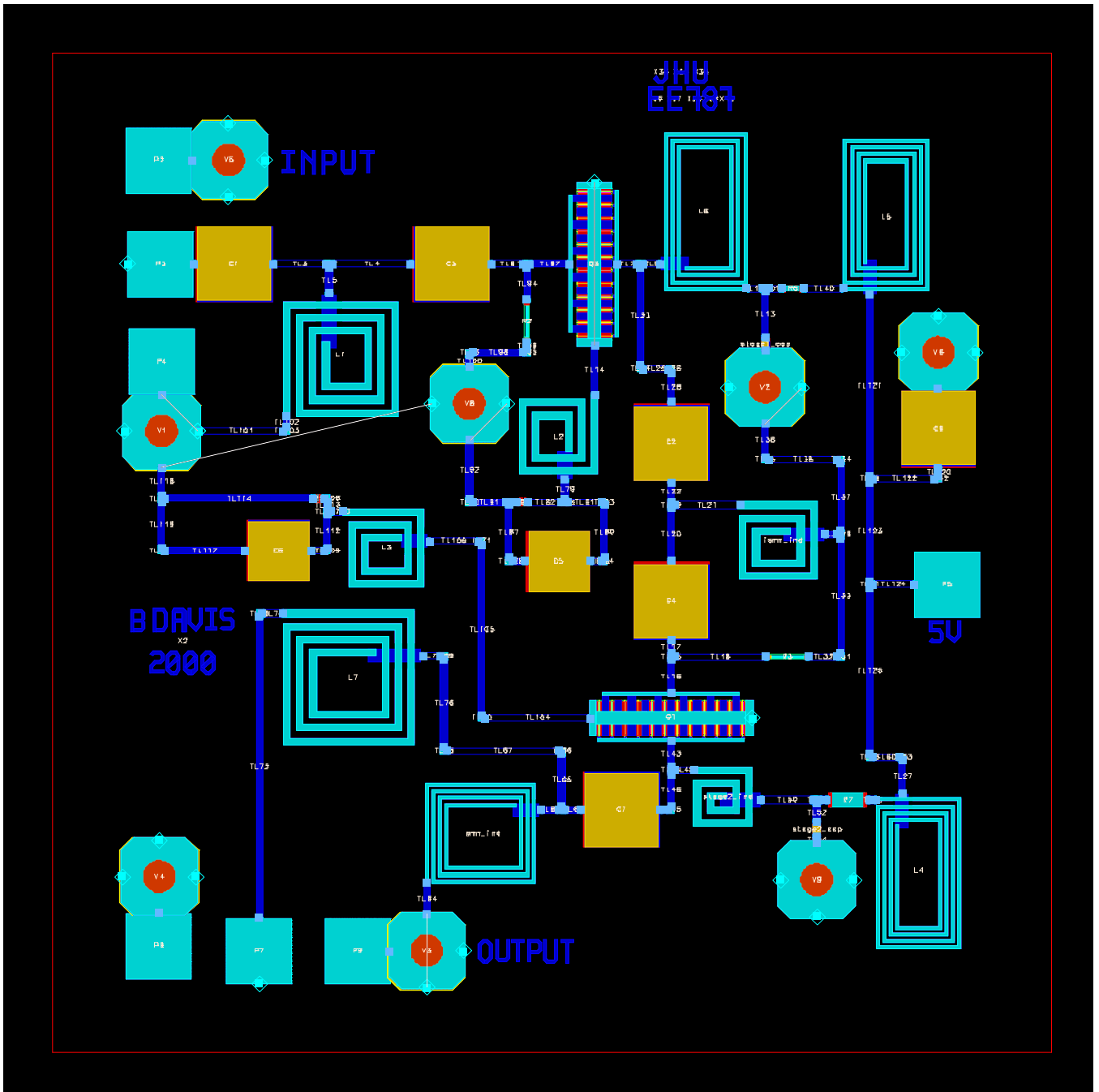


Figure 11 - final layout design

DC Analysis

For verification, the DC Annotation feature of ADS allows the node voltages and currents to be viewed after a simulation. The following figure shows the result of the DC annotations for the first stage of the simplified schematic. The second stage annotation is identical and is therefore not shown. Note that the voltage at the source is 0.216 V. The voltage on the gate is 453 nV or essentially zero. Therefore, the bias on the gate is -0.216 V. This is close to the -0.225 V desired. The current flowing into the drain is 20.6 mA, which is close to the 20.85 mA desired. The voltage on the drain is 2.39 V, which is close to the desired 2 V.

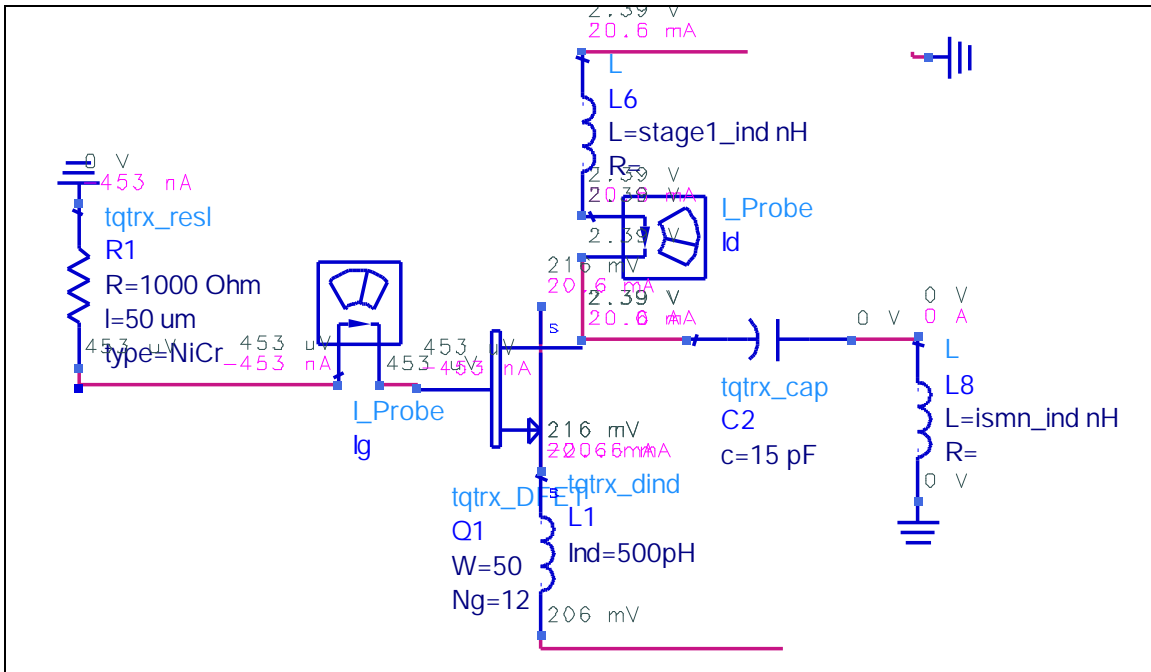


Figure 12 - DC annotation of first stage

The most current flowing in any part of the circuit is 20 mA. All of the interconnects and inductors in the layout circuit are capable of handling this current.

This table summarizes the DC bias check for the simplified schematic.

Table 2 - DC Bias Check Summary

1 st Stage	
Vg = -0.215 V	Vd = 2.39 V
Ig = -0.453 uA	Id = 20.6 mA
2 nd Stage	
Vg = -0.215 V	Vd = 2.39 V
Ig = -0.453 uA	Id = 20.6 mA

Test Plan

To test the chip after fabrication, the following test plans are suggested.

Linear Parameters

To measure the S parameters, a vector network analyzer is needed along with extraction software, preferably Agilent ICCAP. This test plan assumes you have both.

- Calibrate the network analyzer from 0.45 to 10 GHz.
- Using ICCAP, create an extraction module to sweep frequency from 0.5 to 8 GHz in steps of 50 MHz while supplying a bias voltage of 5 volts to the DUT.
- Place the bias probe on the chip's pad that is next to the "5V" indicator.
- Place the probe tips on the appropriate pads. The input port is located on the upper left of the chip and is marked by "INPUT". The output port is located on the bottom left of the chip and is marked by "OUTPUT".
- Begin the ICCAP extraction routine that you have created to measure S parameters and store the data.

Noise Figure

To measure the noise figure, a noise figure meter is needed along with extraction software, preferably Agilent ICCAP. This test plan assumes you have both.

- Calibrate the noise figure meter from 0.45 to 10 GHz.
- Using ICCAP, create an extraction module to sweep frequency from 0.5 to 8 GHz in steps of 50 MHz while supplying a bias voltage of 5 volts to the DUT.
- Place the bias probe on the chip's pad that is next to the "5V" indicator.
- Place the probe tips on the appropriate pads. The input port is located on the upper left of the chip and is marked by "INPUT". The output port is located on the bottom left of the chip and is marked by "OUTPUT".
- Begin the ICCAP extraction routine that you have created to measure noise figure parameters and store the data.

Conclusion and Recommendations

The design was successful and passed all design goals except for gain. In retrospect, the second stage of the amplifier would be redesigned for maximum gain instead of lowest noise figure. The first stage provided a low enough minimum noise figure such that a compromise on the second stage noise figure would have been acceptable and still meet specifications.

The third-order intercept power could not be simulated due to the failure of the harmonic balance simulations. Further investigation into the reason why the design would not simulate is needed.

Appendix – ADS Project File

On the attached floppy diskette is an ADS archive project containing all of the design schematics, plots and layouts used for the design. The file “readme.dsn” describes the various schematics.

Appendix – GDSII (CALMA) Layout File

On the attached floppy diskette is a GDSII layout file for generating the MMIC chip.