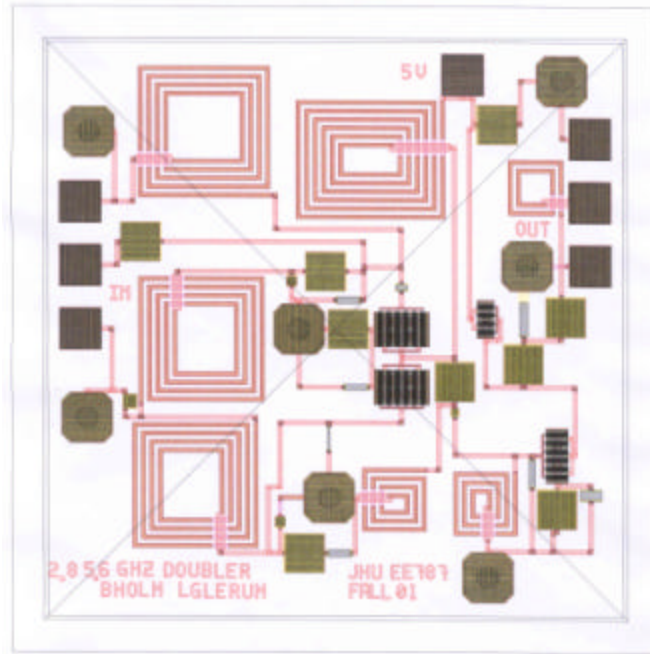


An S/C Band
Frequency Doubler Design
Using Agilent ADS with
TriQuint's Library



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ABSTRACT

This paper details the design of an S/C band frequency doubler on a 60 mil square GaAs MMIC using HP Advanced Design Software and a TriQuint library. This frequency doubler was required to double an input frequency in the range of 2712.5 to 2812.5 MHz to 5424 to 5625 MHz. This frequency doubler is part of a simplex transceiver project for the C-band HiperLAN wireless local area network (WLAN) and the Industrial Scientific, and Medical ISM bands. The center frequency was selected to fall between the WLAN and ISM bands.

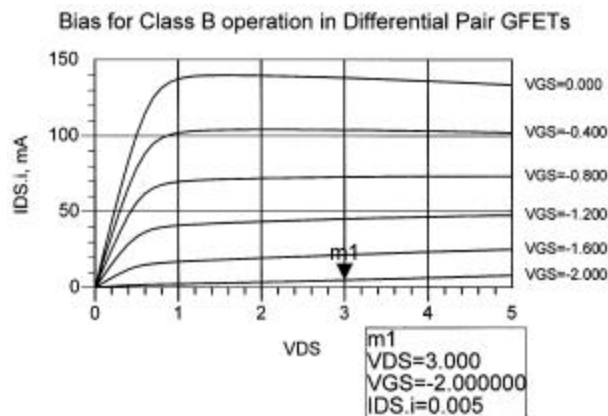
1 INTRODUCTION

1.1 Circuit Description

This MMIC frequency doubler consists of a differential pair of GFET's, a 180 degree phase shift network, and general purpose 2nd stage amplifier. The inputs of the differential pair are fed 180 degrees out of phase by a lumped element 180 degree phase shift network. Each transistor in the differential pair is biased class B that is to have a 50% conduction angle. The output appears as a full wave rectified version of the input, each transistor contributing every other "hump" in the output. Because of the symmetry of the output waveform (it is ideally even symmetric and half-wave even symmetric), it contains no odd harmonics. Therefore, the fundamental and third harmonics normally present in a nonlinear element doubler have been removed by symmetry. A second stage general purpose amplifier provides approximately 6 dB of gain to account for the conversion loss in the differential pair of GFETs.

1.2 Design Philosophy

The first step to designing this frequency doubler was to determine if the differential GFET pair would give the desired 2nd harmonic output while rejecting the 3rd harmonic and fundamental frequencies. A simple schematic consisting of a GFET differential pair with biasing power supplies and an ideal 180 degree transmission line was created and simulated with HP ADS. TriQuint 300 um GFET devices were selected initially since the 300 um device is TriQuint's standard device. A gate to source voltage (V_{gs}) of -2 V that is near the threshold voltage (see figure below) provided good results.



The next step in the design process was to create a 180 degree phase shift network from ideal lumped elements, since the operating frequency is too low for any practical transmission line elements.

To minimize the number of inductors required for a 180 degree lumped element, a double-Pi (two cascaded 90 degree lowpass networks) network was designed for a 50 ohm impedance. When the ideal 180 degree transmission line was replaced with the double-Pi 180 degree lumped element network the frequency doubler still provided good results.

The next step in the design process was replacing the ideal power supply biasing at the gate and drain with a self-bias scheme using a single 5 volt power supply. A large 10 pF shunt capacitor at the power supply and large series inductor of approximately 6000 pH provided adequate RF to DC isolation. Each gate of the differential pair was provided an approximate 0 Volt dc bias through a large resistor to ground. A shared 180 ohm source resistor bypassed with a large 10 pF shunt capacitor provided approximately minus 2.0 volts DC for V_{gs} .

Once proper biasing was obtained, the input matching network (IMN) and output matching networks (OMN) were designed. With the IMN and OMN networks added, the doubler contained a potentially unstable region at approximately 3.4 GHz. This oscillation was traced to a parallel resonance in the double-Pi 180 degree lumped element network. Professor Craig Moore suggested changing the double-Pi 180 degree lumped element network to a 100 ohm impedance and placing 100 ohm resistors at the gates of the differential pair to stabilize the circuit. This change worked very nicely and had the added benefit of a more broadband match at the IMN and OMN when the networks were retuned.

All ideal elements were replaced with TriQuint elements and the circuit was resimulated. This action degraded the performance of the frequency doubler. It was found that the resistive losses in the TriQuint discrete inductors caused a voltage difference between the right and left gates of the differential pair. To account for the resistive losses in the inductor, an 18 ohm series resistor was added at the left gate of the differential pair. The IMN and OMN were also tuned to optimize performance.

At this point in the design process, a rough layout design was performed to ensure that the current circuit would fit on a 60 mil square GaAs MMIC with some room to spare for a 2nd stage amplifier. The circuit layout left about 1/5 of the area for a 2nd stage amplifier which was needed to provide an additional 6 dB gain to reach the goal conversion loss of 0 dB. To fit a second stage amplifier in this area, an active bias network (a half-sized FET with its gate and source connected to create a current source) was selected for the second stage. Furthermore, the IMN and OMN's were kept physically

small by using 200 ohm shunt resistors at the input and output, and by choosing topologies that minimized the amount of inductance required.

1.3 Trade-Offs

The most significant and earliest tradeoff made was the choice of circuit architecture. By using a pair of GFET's driven out of phase for the doubler, it was possible to save a filter that would have been required to block the fundamental and third harmonic created by a more straightforward diode-connected-FET single non-linearity design. Of course, this choice meant it was necessary to construct a phase shift network. It wasn't possible to build both and do a comparison, but the dual transistor approach seemed more novel and elegant, so it was the one chosen. During the layout process, there were numerous small tradeoffs. Individual inductors only come in discrete sizes, so every time our design called for one, we had to add some microstrip line to tune the inductance. And every time we added microstrip line to physically connect things, we had to account for that additional inductance somewhere else. The post-amplifier circuit was designed to be small, not for high performance. Most notably, it has large stabilizing shunt loads on its input and output that made the circuit easier to match to 50 ohms without using large components, especially inductors. It also uses an active load for the bias circuit, which also saves space over that of an inductor used as an RF choke.

2 MODELED PERFORMANCE

2.1 Specifications Compliance Matrix

Characteristic	Specifications	Pre-Layout Results	Final Layout Results
Input Frequency Range	2712.5 – 2812.5 MHz	2712.5 – 2812.5 MHz	2712.5 – 2812.5 MHz
Output Frequency Range	5425 – 5625 MHz	5425 – 5625 MHz	5425 – 5625 MHz
Conversion Loss	3 dB max	5.4 dB	<0 dB
Spurious Fundamental Output	16dBc min, 25 dBc goal	32.8 dBc	39.8 dBc
Spurious 3 rd Order Output	20dBc min, 30 dBc goal	39.8 dBc	35.9 dBc
Input VSWR, 50 Ohms	2.5:1 max, 1.5:1 goal	1.19 max	1.28 max
Output VSWR, 50 Ohms	2.5:1 max, 1.5:1 goal	1.34 max	1.13 max
Supply Voltage	+/- 5 V, +5 V only goal	+5 V only	+5 V only
Size	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP

2.2 Predicted Performance

Figures 1- 3 show the predicted performance of the final layout for the 2.7 - 2.8 GHz frequency doubler.

2.2.1 Output Harmonic Content vs. RF Power In

Figure 1 details the expected output spectrum of the frequency doubler over a swept RF input level.

Marker m2 is the desired doubler output for an input level of +10 dBm. The final layout predicts a conversion gain of approximately 2 dB, and suppression of the fundamental and 3rd order products that exceeds the design goals.

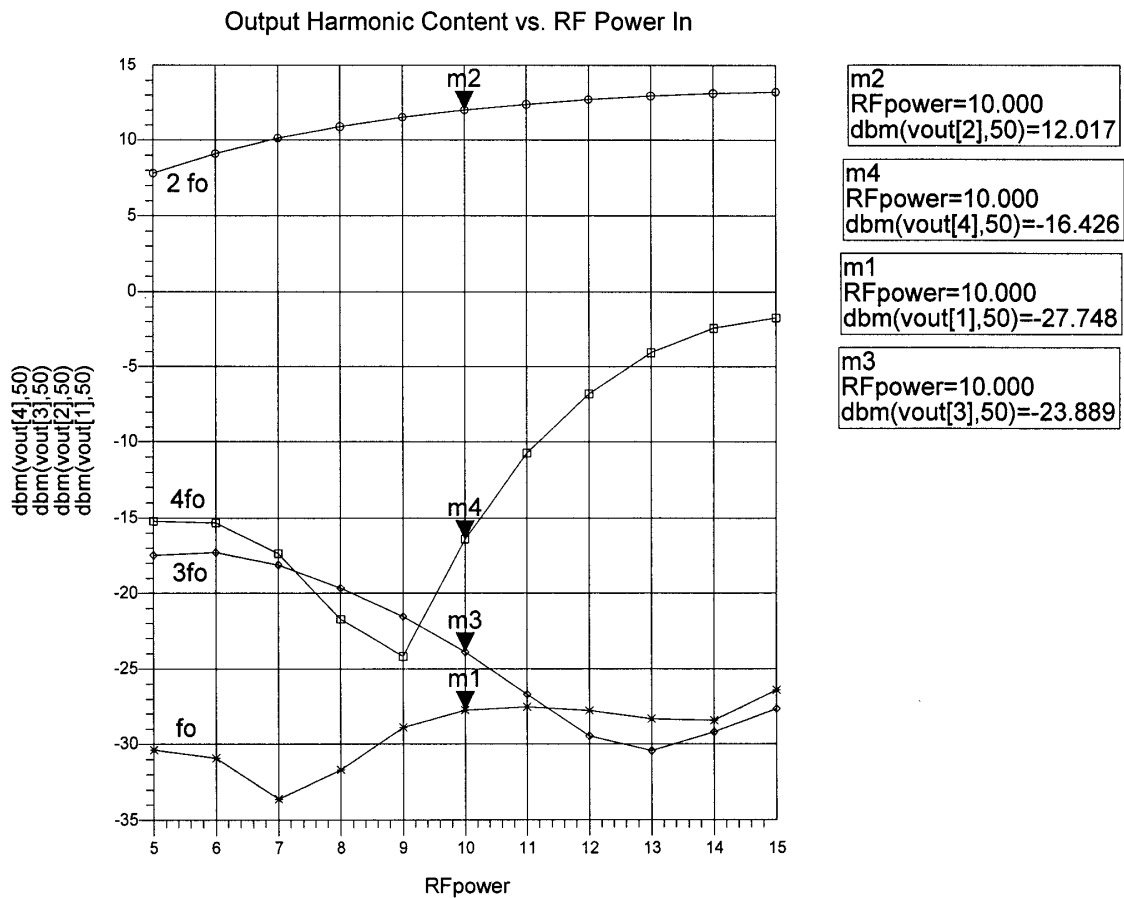


Figure 1

2.2.2 Input and Output Waveforms

Figure 2 shows the time domain representation of the input and output waveforms of the frequency doubler.

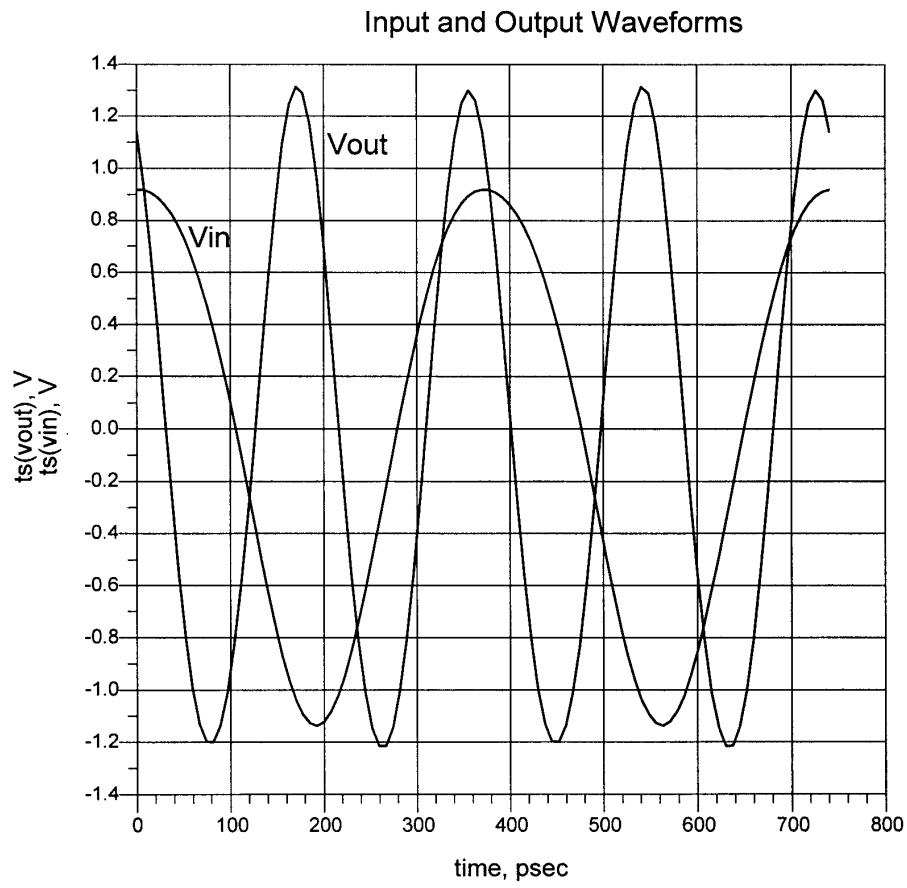


Figure 2

2.2.3 Input VSWR and Output VSWR

Figure 3 shows the predicted VSWR performance of the input and output ports.

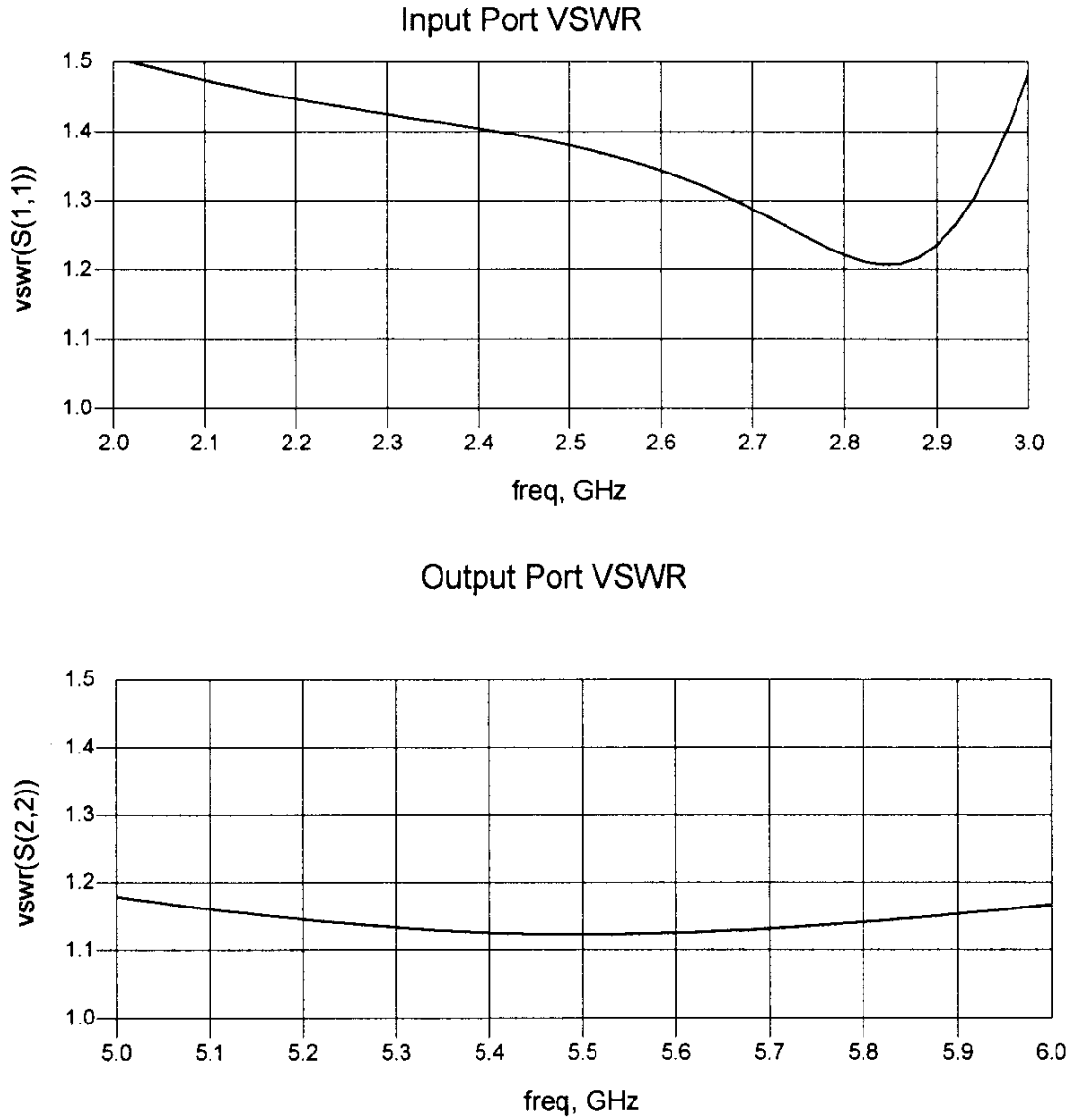
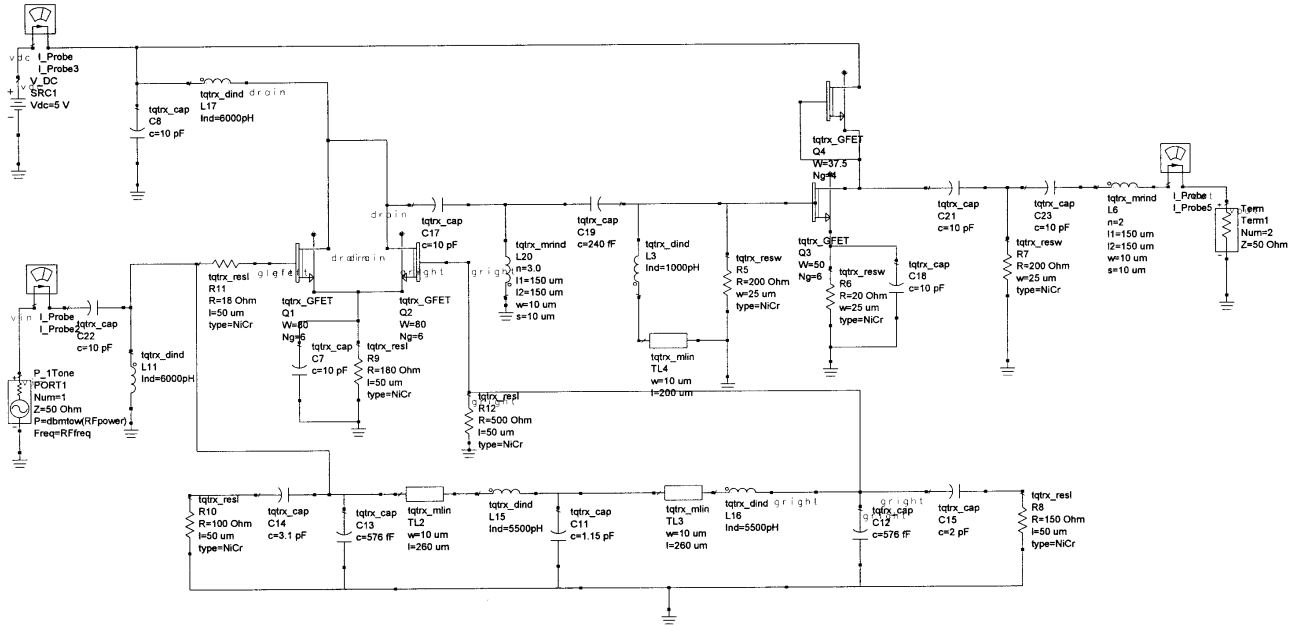


Figure 3

3 SCHEMATIC DIAGRAMS

3.1 Simplified Schematic

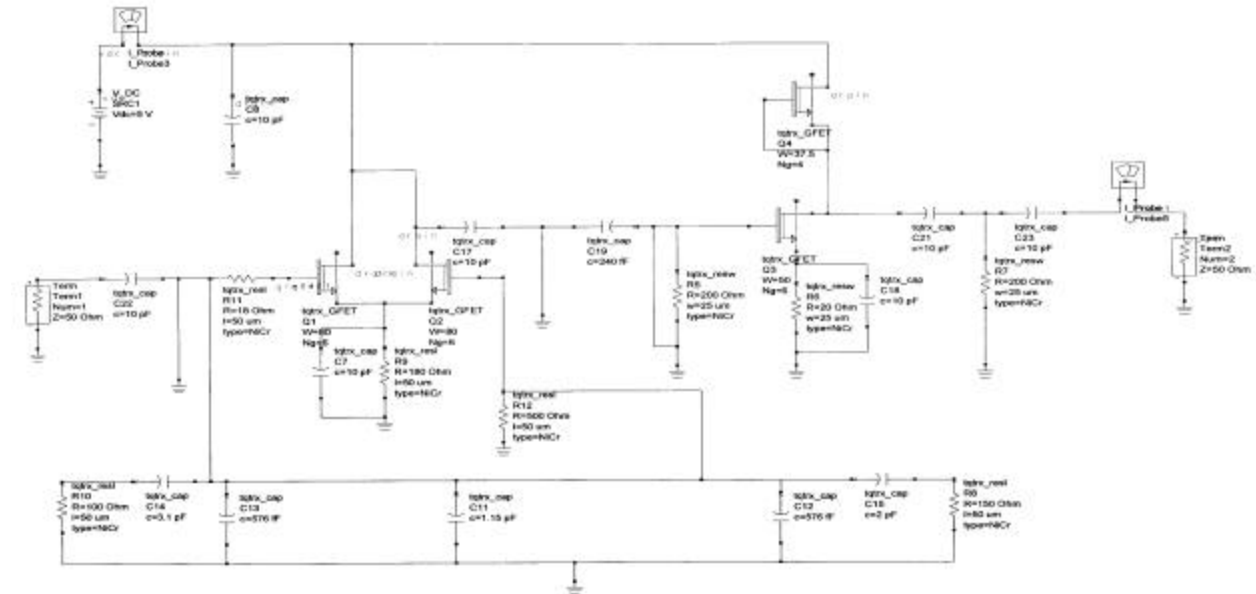
The schematic below has been simplified by removing all routing microstrip lines (bends tees and short MLINs), which did not significantly affect the simulated results.



4 DC ANALYSIS

4.1 DC Schematic

The DC schematic below has been simplified further by replacing inductors and microstrip lines with wires.



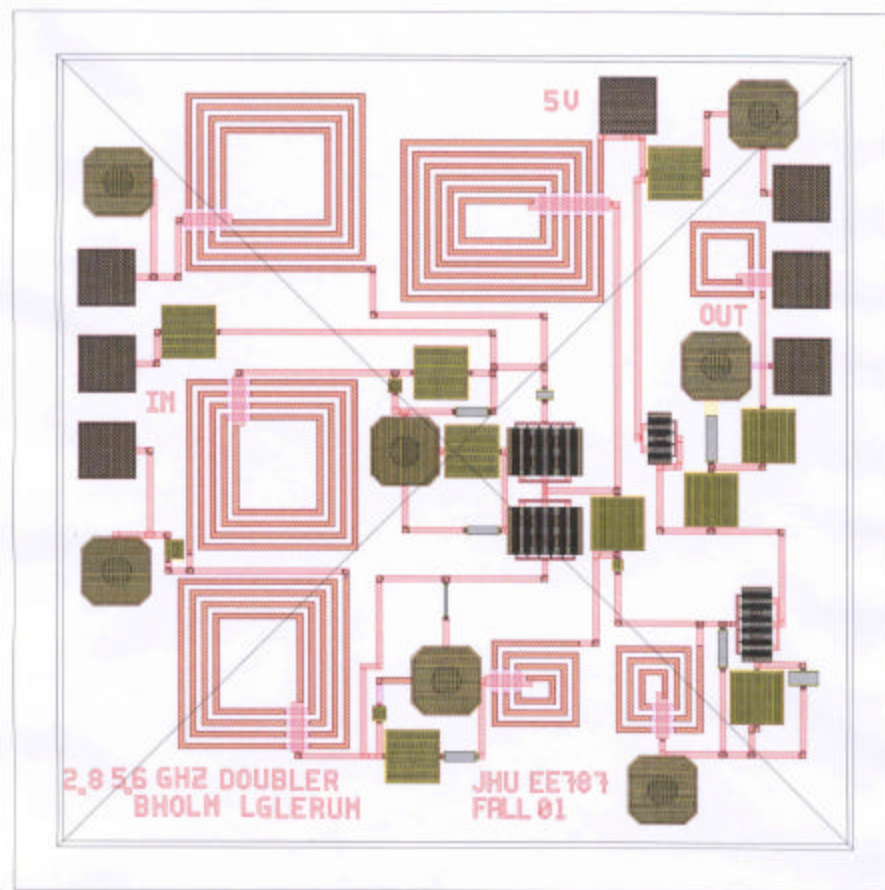
4.2 Bias Check

A bias check was performed on the simplified schematic to ensure that there was no inadvertent DC shorts to ground and that the circuit was biased properly. All biasing was correct, however it was discovered that blocking caps at the input and output ports were inadvertently left out of the schematic.

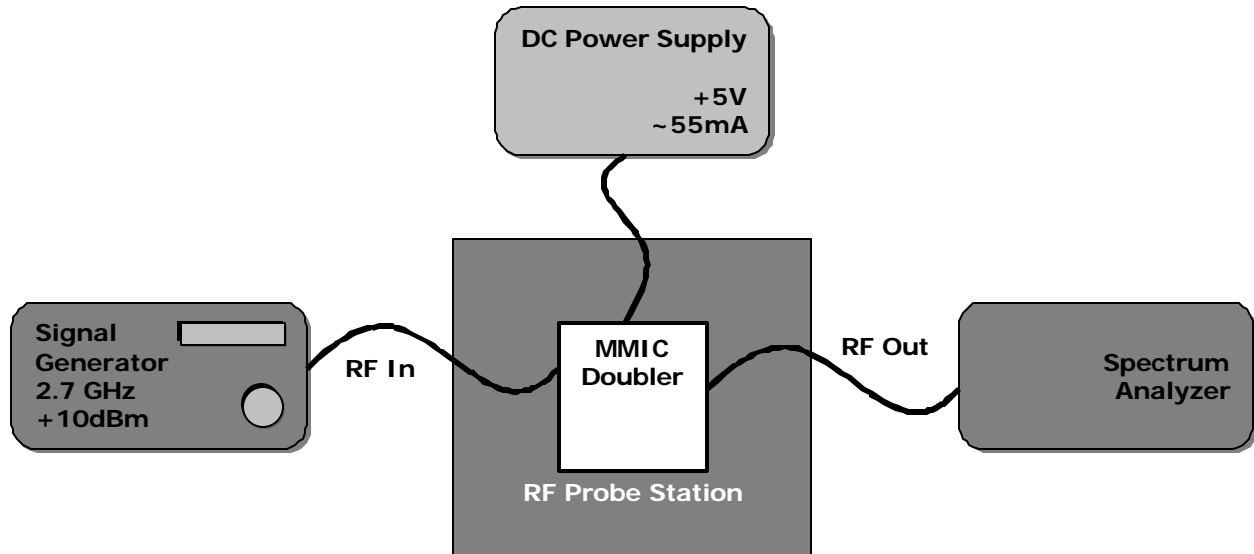
4.3 Interconnect and Component DC Current Stress

In performing the interconnect and component DC current stress analysis, instructors John Penn and Craig Moore discovered that resistor R6 located in series with drain of the output stage amplifier did not have sufficient width to support the current. All other components were satisfactory.

4.4 Final Layout



5 TEST PLAN



Test Equipment Required:

- 1 Glerum/Holm GaAs MMIC Doubler
- 1 RF Signal Generator, 2.7-2.8GHz, +5-15dBm output, (+10dBm minimum)
- 1 Spectrum Analyzer, 1-12GHz (6 GHz minimum). Power out of device could exceed +15dBm, use attenuator if necessary.
- 1 DC Power Supply (+5Vdc, 100mA) with DC milliammeter
- 1 Needle Probe for DC bias
- 2 RF Ground-Signal-Ground Probes

Test Plan:

1. **Visual Inspection.** Verify the chip's identity against the paper printout and check for obvious physical defects. Look for missing elements, inverted components, and chips and cracks.
2. **Bias Current Test.** With power supply off and set to 0V, connect the supply leads to the MMIC doubler chip. Turn supply on and slowly raise the voltage toward +5V. Monitor the current and shut the supply off if it goes above 70mA. (55mA is predicted draw.) Record the actual current draw here _____mA.
3. **RF Connections.** Install MMIC in RF test fixture with its text oriented right side up. Connect the RF input on the left and the RF output on the right.
4. **Functional Test.** Turn on the signal generator and set it to +10dBm, 2.7GHz. Verify that there is a $2F_0$ component on the spectrum analyzer within ~6dB of the input level.
5. **Swept Power Test.** Sweep the input power from +5dBm to +15dBm in 1dB steps and note the power in the frequency doubled term for each step. Also note the power in the fundamental, third, and fourth harmonics. Graph the results and compare them to theoretical.
6. **Input and Output Match.** If time permits, use a network analyzer to check the input impedance around 2.7-2.8GHz and the output match around 5.4-5.6GHz. Compare to theoretical.

6 CONCLUSION AND RECOMMENDATIONS

Using a differential pair of GFETs in class B operation proved to be good topology for a frequency doubler when proper balance was maintained. Careful selection of the bias point near cutoff is required such that each transistor only conducts for 180 degrees of the input wave. The double-Pi 180 degree lumped element network had the potential to cause instability in the differential pair when it was originally designed for an impedance of 50 ohms. By designing the double-Pi 180 degree network for a 100 ohm impedance and placing 100 ohm resistors to ground at each end of the network, the circuit was made stable. Further tweaking of the first and last series capacitors in the double-Pi 180 degree network allowed tuning to ensure a 180 degree phase shift.

When laying the frequency doubler schematic out using Agilent ADS several common mistakes could have been avoided. It is recommended to carefully consider placement of inductors. Try to allow for at least 50 mils of space between an inductor and other microstrip lines, vias, or other inductors. Also try to keep a spacing of 60 mils between capacitors and vias. The instructors caught most of the errors in the initial frequency doubler layout using a Design Rule Check (DRC) program.