C-Band Low Noise Amplifier (LNA)

Final Report

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1.0 Summary

A Low Noise Amplifier (LNA) operating at C-Band (5150 to 5875 MHz) has been designed as part of a project for the MMIC Design course at the Johns Hopkins University. The project is a simplex transceiver for the C-band HiperLan wireless local area network (WLAN) operating at industrial, scientific, and medical (ISM) frequencies. The LNA is one of nine unique designs that make up the ten chip C-band transceiver. Each design is contained on a 60 mil square ANACHIP die using the TriQuint TQTRx design process. The design software used was Agilent Advanced Design System 1.5 (ADS). The predicted LNA design achieved all design goals including gain greater than 15 dB (15.4 dB minimum), noise figure less than 3 dB (1.7 dB maximum), input IP3 greater than +5 dBm (+20 dBm), and input/output VSWR goal of 1.5. The final LNA design will be fabricated and tested within the next six months of 2002.

2.0 Introduction

A Low Noise Amplifier (LNA) operating in C-Band (5150 to 5875 MHz) has been designed as part of a project for the MMIC Design course at the Johns Hopkins University. The project is a simplex transceiver for the C-band HiperLan wireless local area network (WLAN) operating at industrial, scientific, and medical (ISM) frequencies. The LNA is one of nine unique designs that make up the ten chip C-band transceiver. Figure 1 is the C-Band transceiver chip set with LNA shown highlighted.

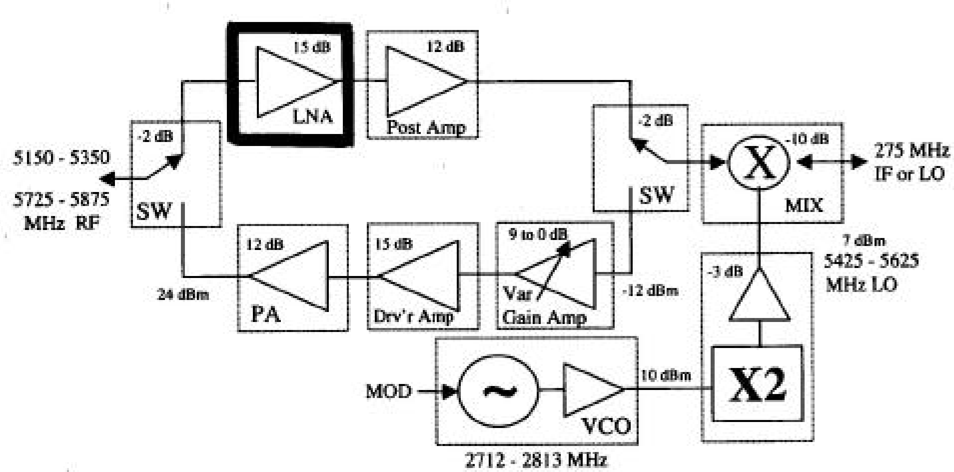


Figure 1. Chip Set for the 5150 – 5350 MHz WLAN and 5725 – 5875 MHz ISM Bands

2.1 Circuit Description

The LNA circuit design selected was a cascaded two-stage amplifier. Both stages utilized 600µm DFETs (12 fingers X 50µm). Self-biasing was used for both stages resulting with a single 5-volt voltage supply. An inductor at the DFET source was used for stabilization. Feedback and high pass filter input matching networks at the second stage achieved broadband performance for gain, noise figure and VSWR.

2.2 Design Philosophy

The TriQuint DFET was selected for the LNA based upon its low noise and gain characteristics. Achieving 15 dB gain with two stages was accomplished by using 600µm DFETs. The 600µm

DFETs resulted with a simpler input matching network for the first stage and higher output power for the second stage.

The design process was focused on achieving a stable design for the design goals of high gain, low noise figure, and input/output VSWR for the required frequency band. A concern throughout the design was predicting a reliable noise figure. The nonlinear DFET transistor model does not yield accurate noise figure data. Representative noise figure data was obtained by using S2P data files for linear models. The final design required switching back and forth from the nonlinear to linear models to obtain reliable noise figure data.

The design process was started by using ideal elements without any concern given to bends, tees, MLINs or real TriQuint elements that would be required for the layout of the final design. This approach was useful for determining the nominal DFET bias points, however numerous iterations and component value changes had to be made for the final layout. The bias points chosen for the final layout were:

Input Stage	Output Stage
Vd = 3.18V	Vd = 4.85V
Vgs = -0.27V	Vgs = -0.29V
Ids = 17.46mA	Ids = 18.58mA

The design started by determining the input matching network for the first stage. Next the network that would be the output matching network for the first stage and the input matching network for the second stage was determined. The required broadband performance of the LNA significantly influenced this network's design. A high pass filter type circuit evolved that gave acceptable broadband performance. Broadband performance was further improved by using feedback for the second stage. Design for the second stage output matching network followed. This composite design using ideal elements was then optimized. Finally, the ideal elements were replaced with TriQuint elements and the design was again optimized. After this step, the layout process was started.

The layout process involved interconnecting appropriate bends, tees, and MLINs to the optimized LNA design with TriQuint elements. General design guidelines included: keeping the separation between components and tracks to at least 3 line widths, sharing vias as much as possible, use of a single power supply and adhering to the minimum allowable resistor width of 1µm per 1ma current through the resistor. This process required going back and forth from the layout to the schematic to simulate and re-optimize performance. Numerous iterations were made to adjust component values to account for layout modifications.

2.3 Trade-offs

The major trade-off was between gain and noise figure. The lower noise figure resulted with less gain. The input VSWR was also compromised somewhat in order to order to meet the gain and noise figure goals. Also the small ripple for the gain across the entire band lowered the gain, raised the noise figure, and increased the VSWR.

3.0 Modeled Performance

3.1 Specification Compliance Matrix

Table 1 itemizes the design specifications and the predicted performance for the LNA.

Table 1. LNA Specification Compliance Matrix

Characteristic	**Specification Goal**	**Simplified Schematic (no bends, tees, or MLINs)**	**Final Layout Predicted Performance**
Frequency	5150 to 5875 MHz	5150 to 5875 MHz	5150 to 5875 MHz
Bandwidth	>725 MHz	-	800 MHz
Gain	>15 dB	12.8 dB	15.5 dB
Gain Ripple	±0.5 dB	±1.6 dB	±0.5 dB
Noise Figure	<5 dB, 3 dB goal	2.14 dB	1.74 dB
Input IP3	>+5 dBm	-	+20 dBm
VSWR, 50 Ohm	<1.5:1 (14 dB) input & output	-6.9 dB input -9.8 dB output	-14.2 dB input -15.2 dB output
Supply Voltage	+5 Volts only, goal	+5 Volts, one supply	+5 Volts, one supply
Size	60 X 60 mil ANACHIP	-	60 X 60 mil ANACHIP

3.2 Predicted Performance

The following plots included in this report show the characteristics and predicted performance of the LNA design.

Figure 2. LNA Simplified Schematic S-Parameters
Figure 3. LNA Simplified Schematic Stability Plot
Figure 4. LNA Final Layout Schematic S-Parameters*
Figure 5. LNA Final Layout Schematic Noise Figure (Linear DFET S2P file)
Figure 6. LNA Final Layout Schematic Stability Plot
Figure 7. LNA Final Layout Schematic Input IP3 Plot

* Figures 4 to 8 are for the LNA final layout schematic with bonding wires at the input, output and 5 volt supply.

Figure 2. LNA Simplified Schematic S-Parameters

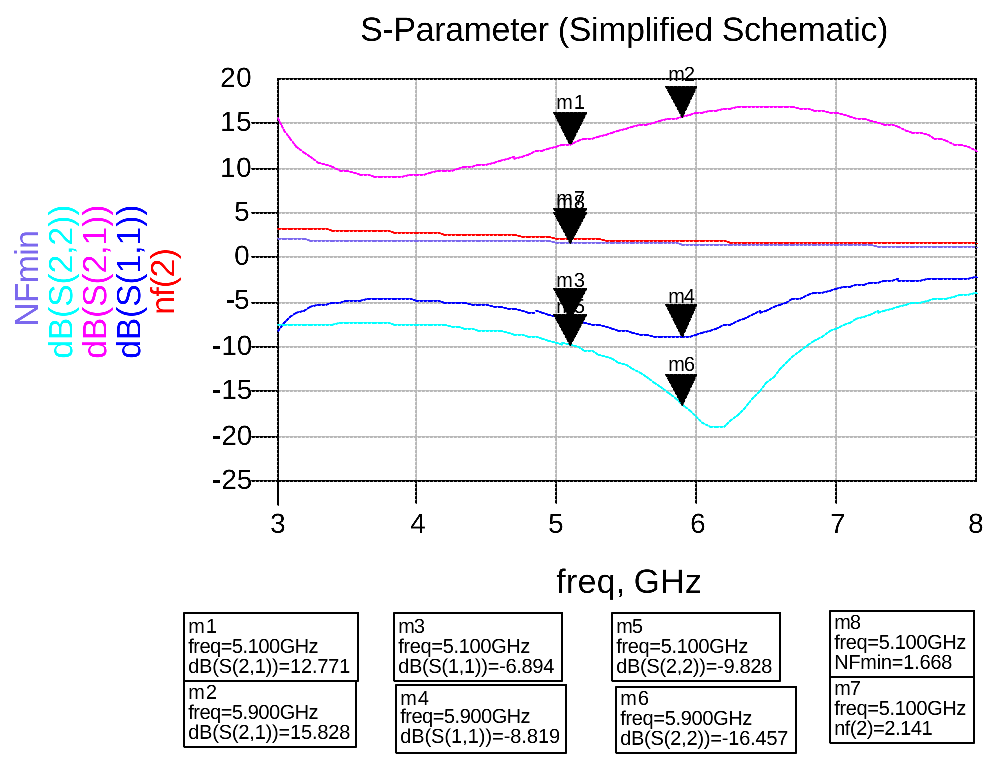


Figure 3. LNA Simplified Schematic Stability Plot

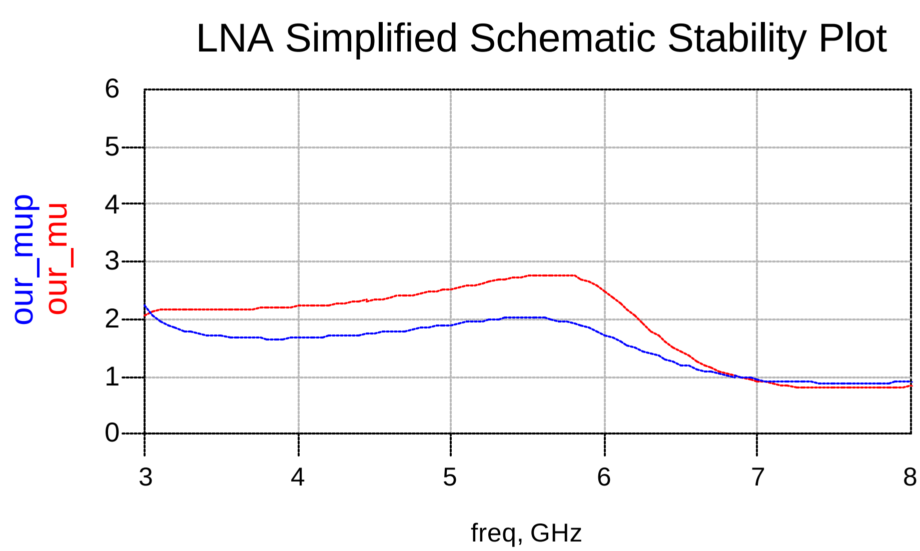


Figure 4. LNA Final Layout Schematic S-Parameters

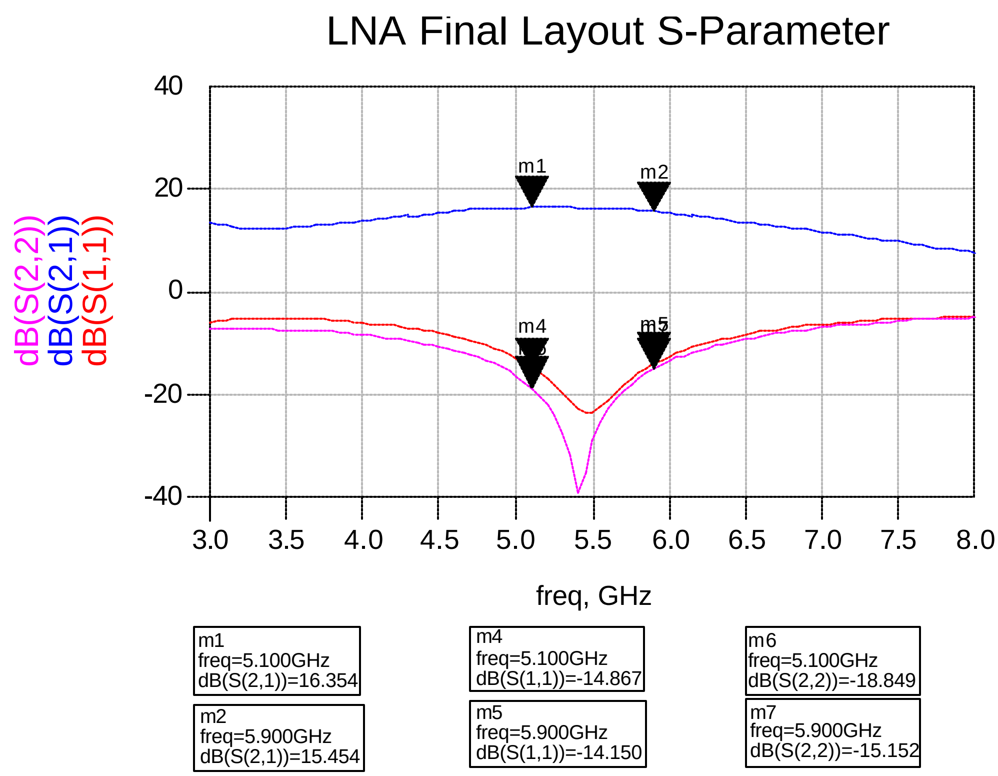


Figure 5. LNA Final Layout Schematic Noise Figure (Linear DFET S2P file)

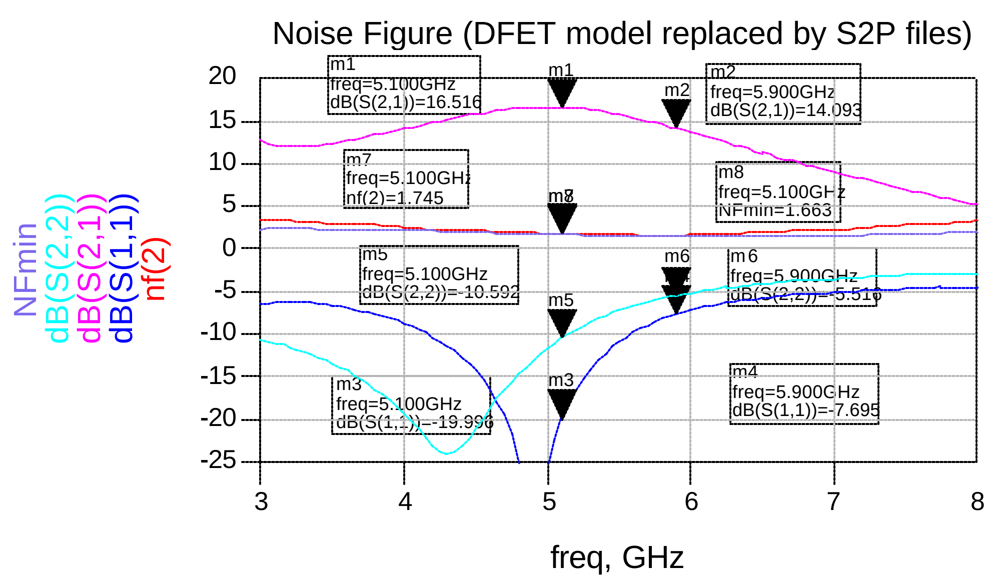


Figure 6. LNA Final Layout Schematic Stability Plot

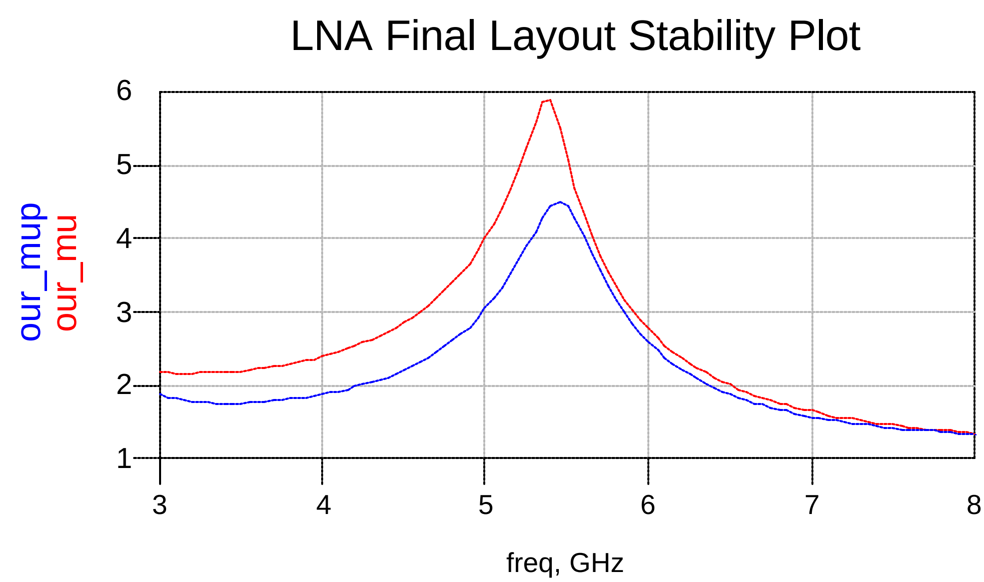
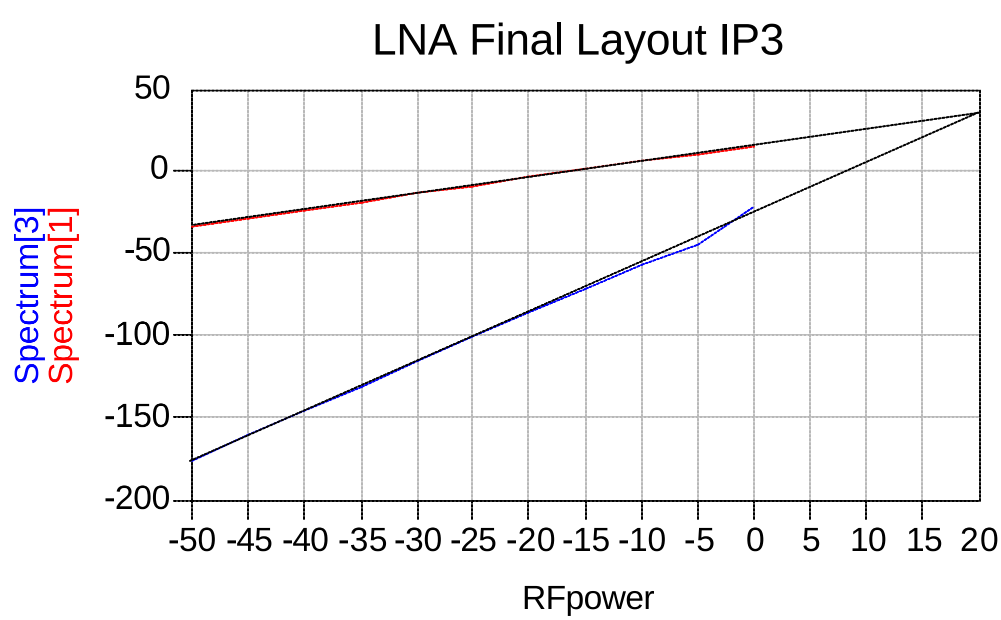


Figure 7. LNA Final Layout Schematic Input IP3 Plot



4.0 Schematic Diagrams

The following schematics are included in this report.

Figure 8. LNA Simplified Schematic
Figure 9. LNA Final Layout Schematic
Figure 10. LNA Final Layout Schematic with DFET model replaced by S2P file
Figure 11. LNA Final Layout in ANACHIP

5.0 DC Analysis

For the input and output stages, Vd, Vgs and Ids were selected for the maximum gain and lowest noise figure that could be achieved simultaneously. Table 2 summarizes the DC bias check for the LNA.

Table 2. DC Bias Check

Input Stage	Output Stage
Vd = 3.18V Vgs = -0.27V Ids = 17.46mA	Vd = 4.85V Vgs = -0.29V Ids = 18.58mA

The currents through all resistors were checked to verify that the resistor widths selected adhered to the layout guidelines. The guideline followed was that the minimum allowable resistor width be1µm per 1ma current through the resistor. In particular, the 100 ohm voltage dropping resistor for Ids of the first stage was 25µm and drew 18ma. Also the first and second stage 15 ohm source resistors were 25µm and drew 18ma. The feedback resistor for the second stage was 5µm and drew only 1.3µa.

Figure 12 is the simplified schematic showing the voltages and currents throughout the layout.

Figure 8. LNA Simplified Schematic

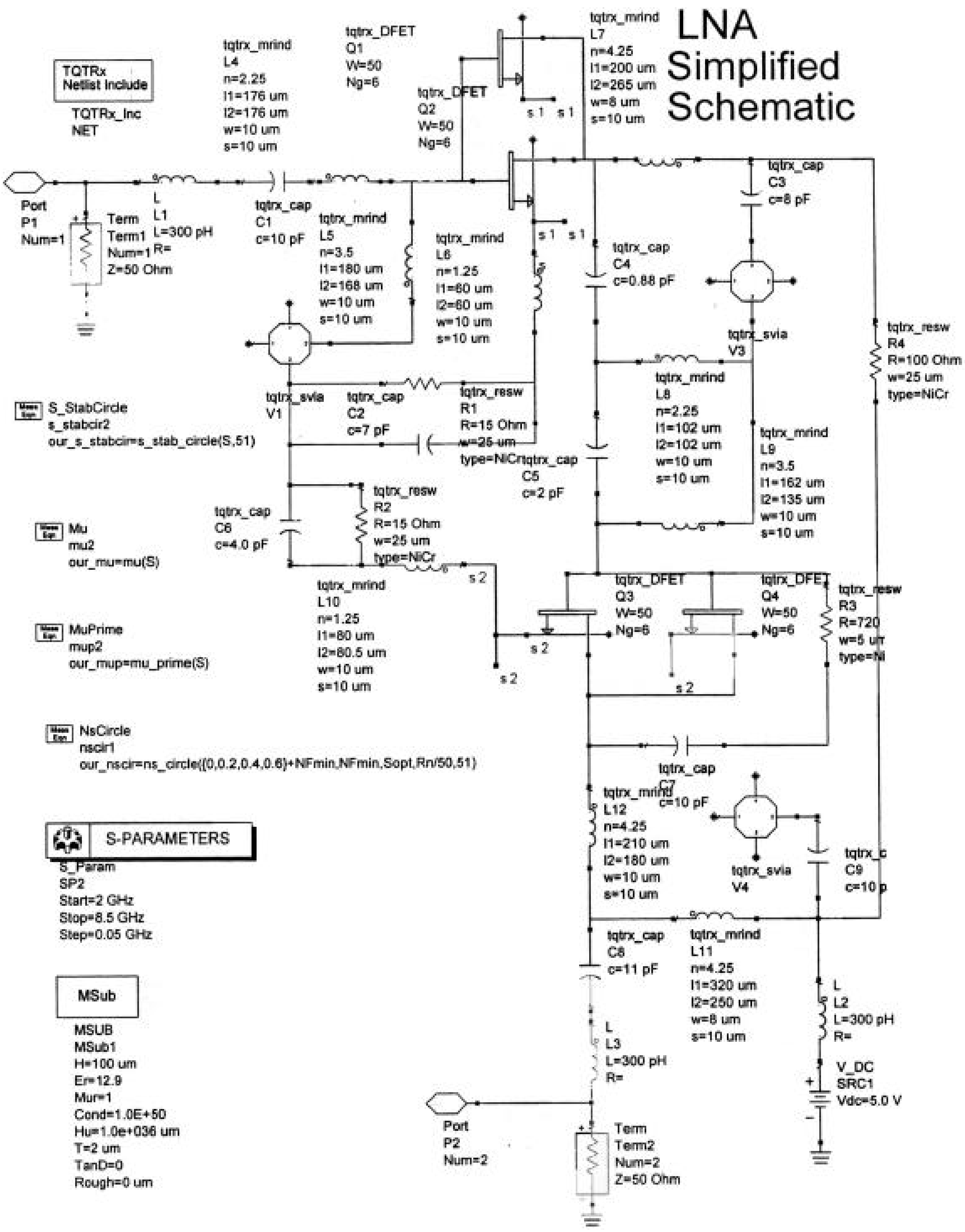


Figure 9. LNA Final Layout Schematic

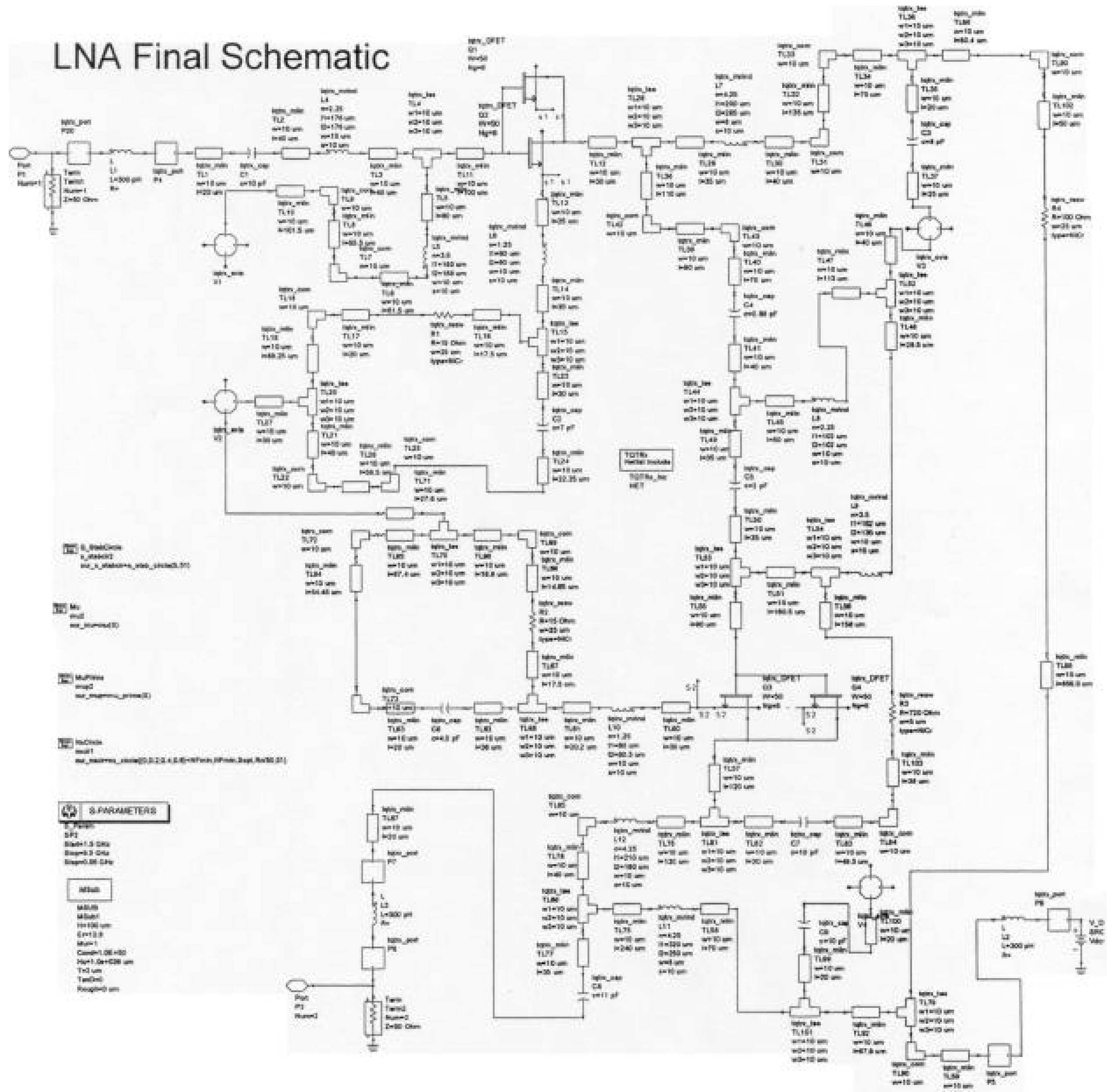


Figure 10. LNA Final Layout Schematic with DFET model replaced by S2P file

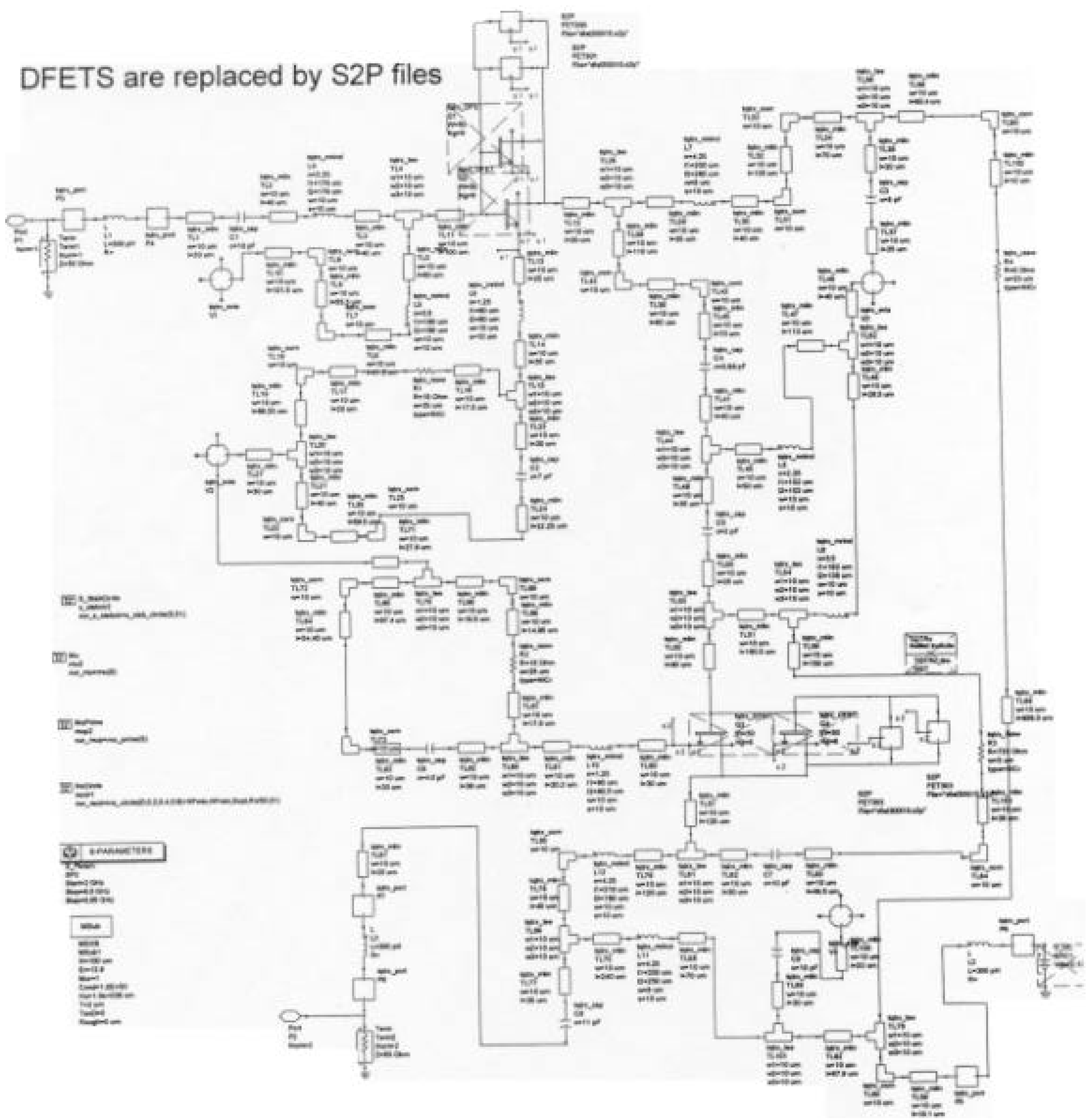


Figure 11   LNA Final Layout in ANACHIP

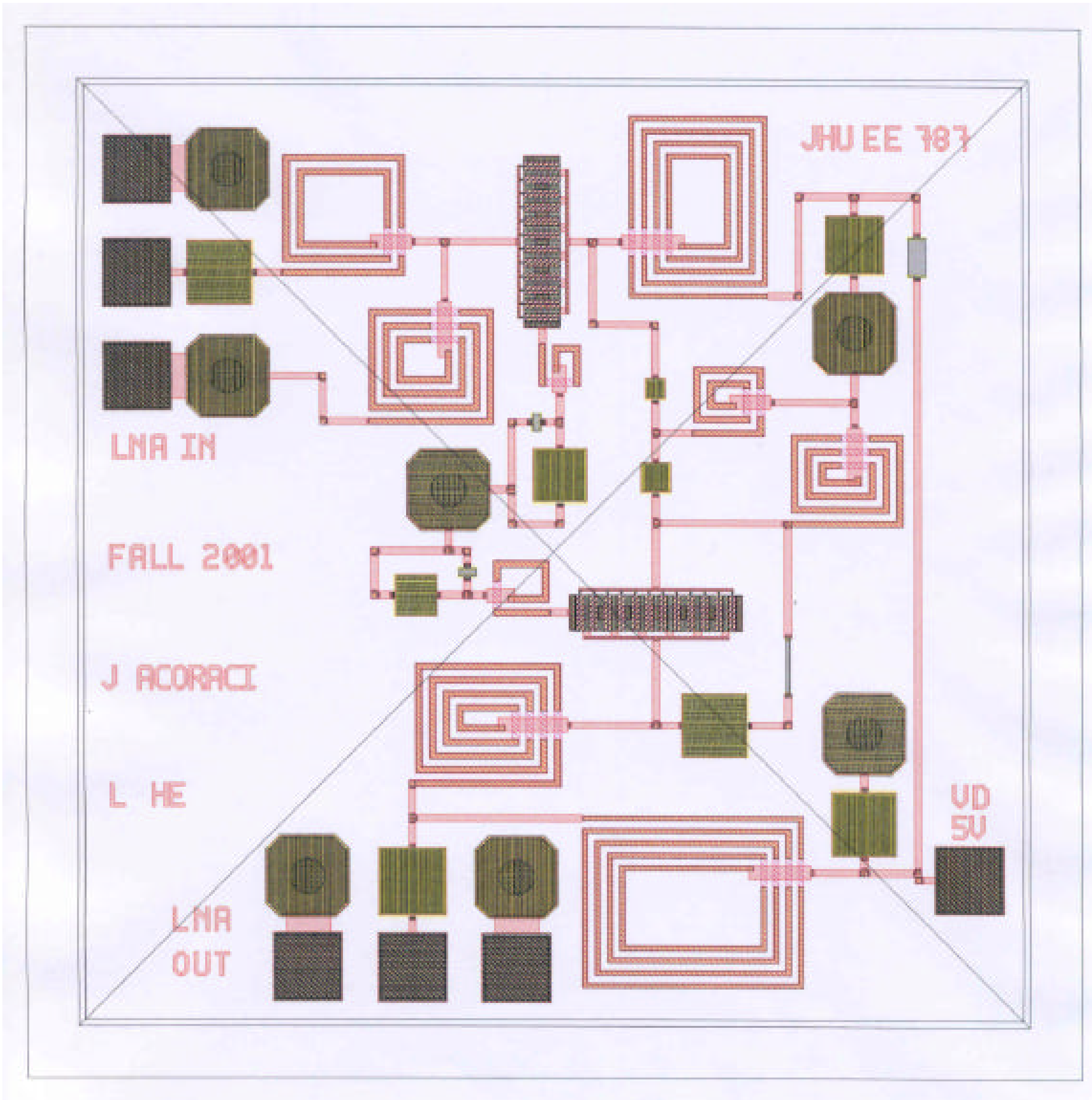
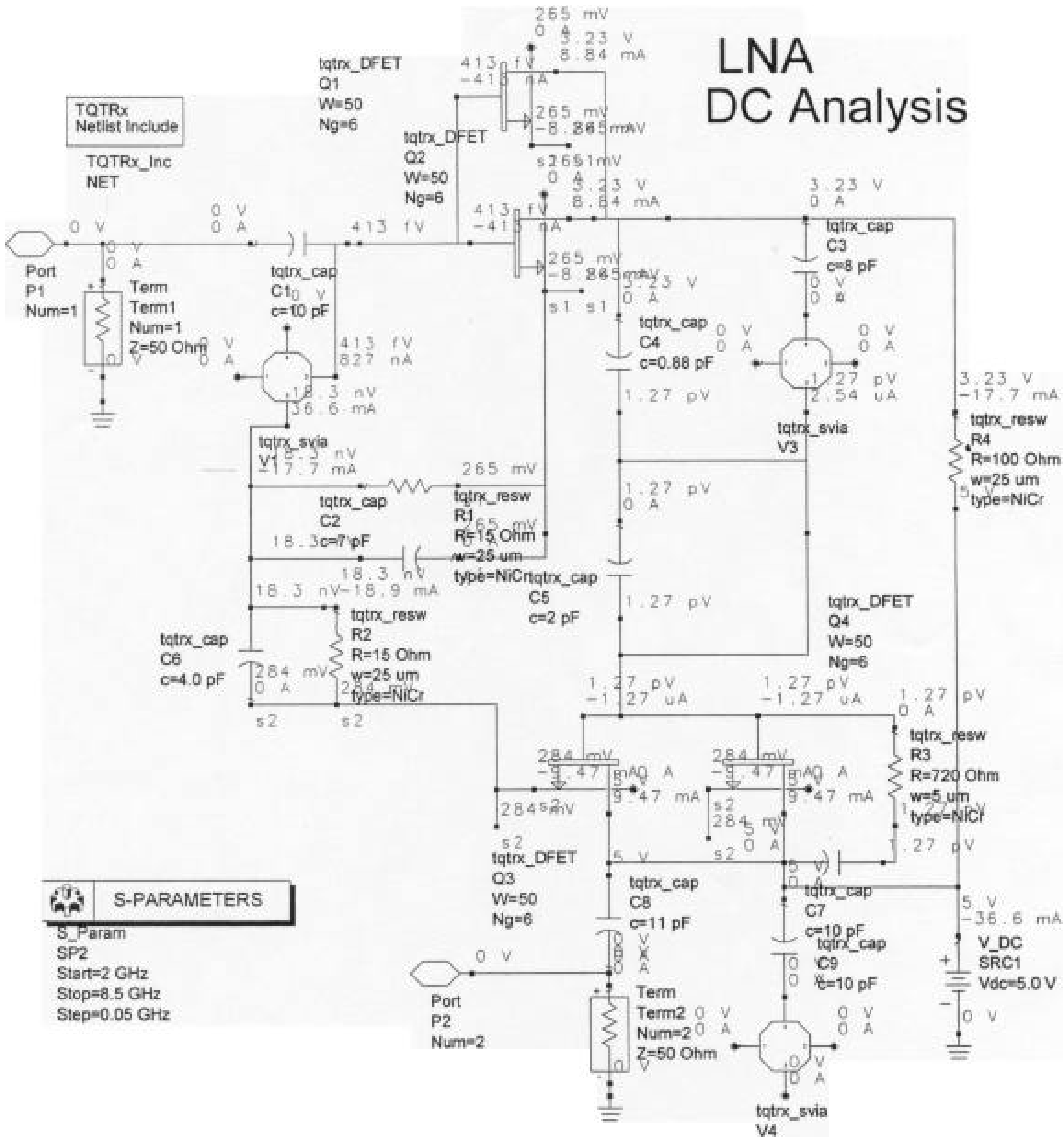


Figure 12. Simplified DC Schematic



6.0 Test Plan

6.1 Test Equipment

The following test equipment or equivalent is necessary to measure the LNA performance:

- Agilent 8510 Network Analyzer
- Agilent XXX Noise Figure Meter
- 5 volt DC power supply

6.2 Turn On Procedure

Extreme caution should be taken when turning on the 5 volt DC powers supply so as not to draw excessive current.

- The required voltage for the LNA is **+5 V DC**
- The required current for the LNA is **36.04 mA**

6.3 S-Parameter Measurement

- Calibrate the network analyzer from 1 to 10 GHz
- Position the bias probe on the "VD 5V" pad
- Position the input probes on the "LNA IN" input pads
- Position the output probes on the "LNA OUT" pads
- Make S11, S21, S12, S22 measurements and store all data on disk

6.4 Noise Figure Measurement

- Calibrate the noise figure meter
- Position the bias probe on the "VD 5V" pad
- Position the input probes on the "LNA IN" input pads
- Position the output probes on the "LNA OUT" pads
- Make noise figure measurements and store all data on disk

7.0 Conclusion and Recommendations

The LNA design process was very successful in that all design goals were met. In particular the noise figure of 1.7 dB was much lower than the goal of 3 dB. Also the input IP3 of +20 dBm was much higher the goal of +5 dBm. A recommendation to be more efficient in the design process is to spend less time with the ideal element design and more time with the TriQuint elements and the real layout with bends, tees, and MLINs.

8.0 Project File

The project file has been submitted on a 3 ½ HD Diskette.

9.0 GDSII (CALMA) Layout File

The GDSII layout file has been submitted on a 3 ½ HD Diskette